

EXHIBIT 2

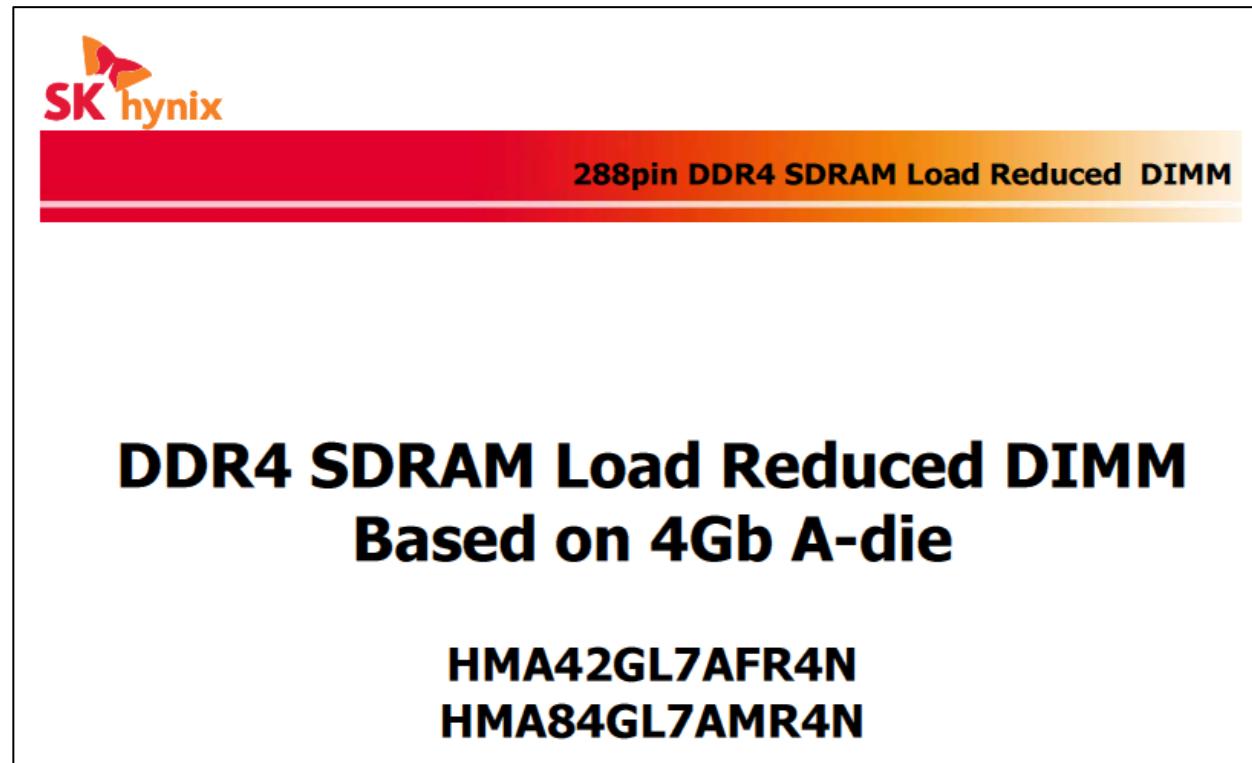
U.S. Patent No. 10,217,523
SK hynix HMA84GL7AMR4N-UHTE

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"

1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:	<p>The SK hynix Products are memory module accessible in a computer system by a system memory controller via a system memory bus.</p> <p>For example, the SK hynix Products are DDR4 load reduced dual in-line memory modules ("LRDIMM").</p>
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(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).



"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"

SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet, at 1.



Description

SK hynix Load Reduced DDR4 SDRAM DIMMs are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Load Reduced DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

Features

- 288 pin Load Reduced DDR4 DRAM Dual In-Line Memory Modules
- Buffer performance by LRDIMM presenting less load to system

See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 3 (annotation added).

JEDEC Standard No. 21C
Page 4.20.27-1

4.20.27 - 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/
PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification

DDR4 SDRAM Load Reduced DIMM Design Specification

Revision 1.00

August 2015

See JEDEC LRDIMM Specification.

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"

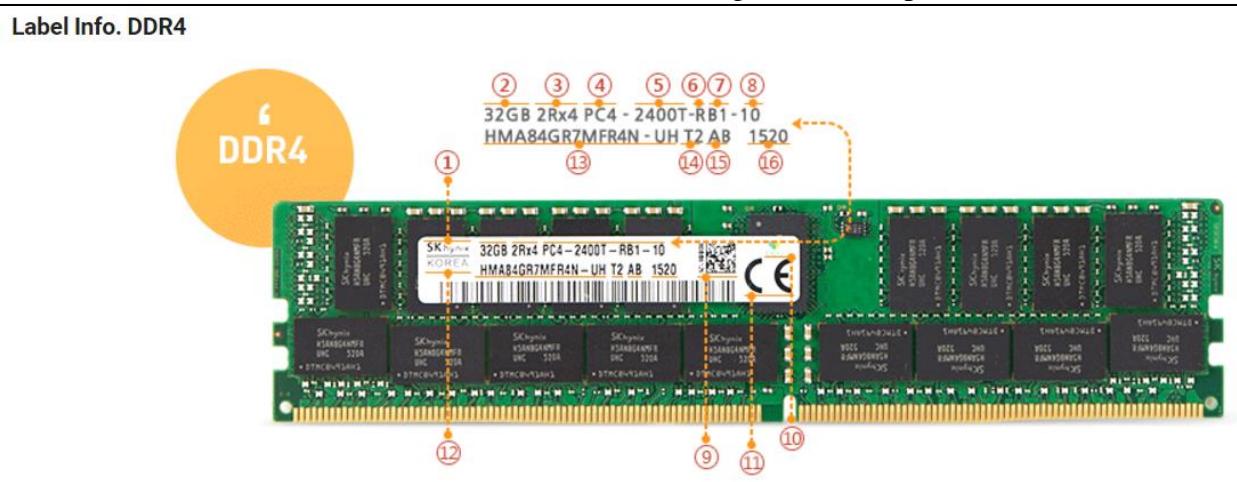
JEDEC Standard No. 21C
Page 4.20.27-5

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.

See JEDEC LRDIMM Specification (annotation added).

The SK hynix HMA84GL7AMR4N-UHTE is manufactured according to JEDEC specifications:



See SKH DDR4 Module Label Info at 3.

(6)	Module Type	U : 288pin Unbuffered DIMM R : 288pin Registered DIMM S : 260 pin Unbuffered SO-DIMM L : 288pin LRDIMM N : 288pin NVDIMM
(7)	Gerber Revision	JEDEC Reference design file used for this design
(8)	SPD Revision	JEDEC SPD Revision Encoding and Additions level

See SKH DDR4 Module Label Info at 3.

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).

DDR4 Load Reduced DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
D0	PC4-LRDIMM_V050_RC_D0_20130828.brd	PC4-LRDIMM_V050_RC_D0_20130828_BOM.xlsx
D1	PC4-LRDIMM_V070_RC_D1_20141106.brd	PC4-LRDIMM_V070_RC_D1_20141106_BOM.xlsx
D2	PC4-LRDIMM_RC_D2_R050_V200_20160229.brd	PC4-LRDIMM_RC_D2_R050_V200_20160229_BOM.xlsx

See JEDEC Annex D - Raw Card D at 1.

The SK hynix Products are intended for use as main memory in computer systems such as servers and workstations.

JEDEC Standard No. 21C
Page 4.20.27-5

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.

JEDEC LRDIMM Specification (annotation added).

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"



Description

SK hynix Load Reduced DDR4 SDRAM DIMMs are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Load Reduced DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 3 (annotations added).

The SK hynix Products are accessible in a computer system by a system memory controller via a system memory bus. For example, the SK hynix Products include a printed circuit board (PCB) for communicating signals between (e.g., to/from) the memory module and the memory controller of a host system via a bus.

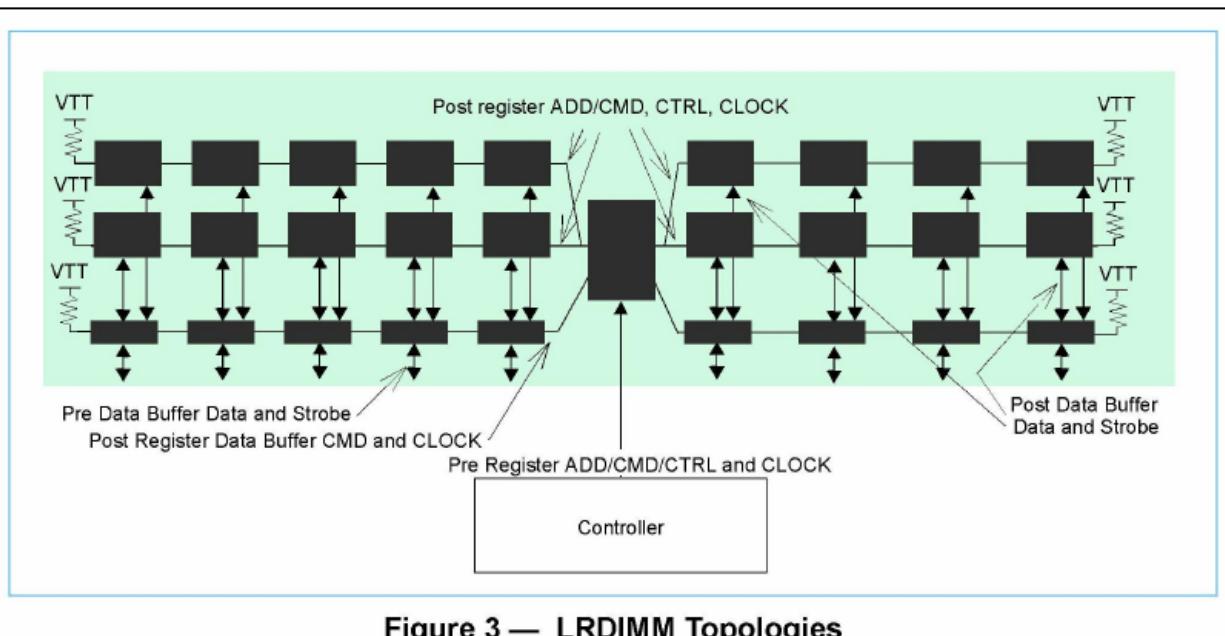


Figure 3 — LRDIMM Topologies

JEDEC LRDIMM Specification.

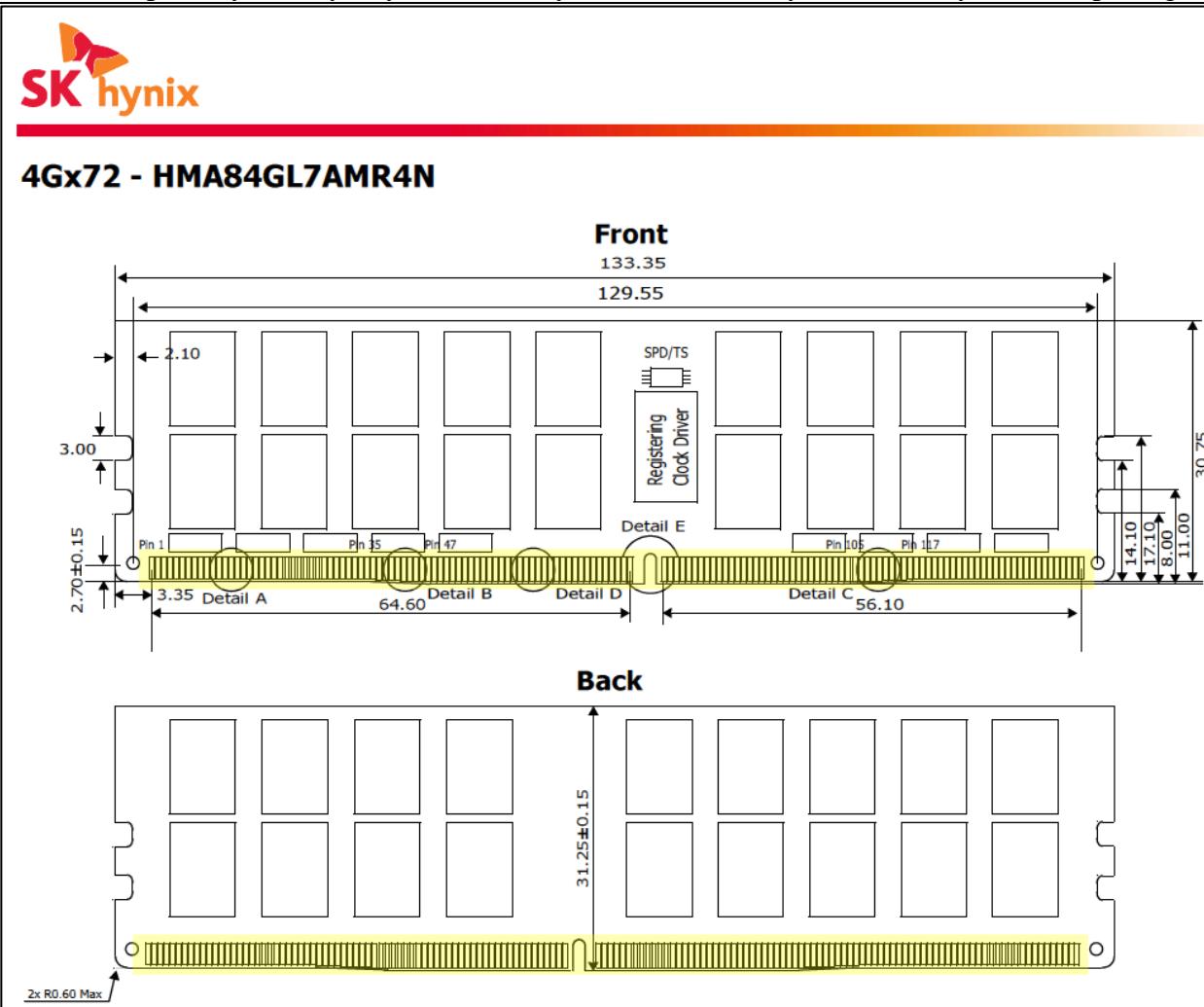
For example, the SK hynix Products contain contacts for connecting to a memory controller of a computer system.

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE)

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"



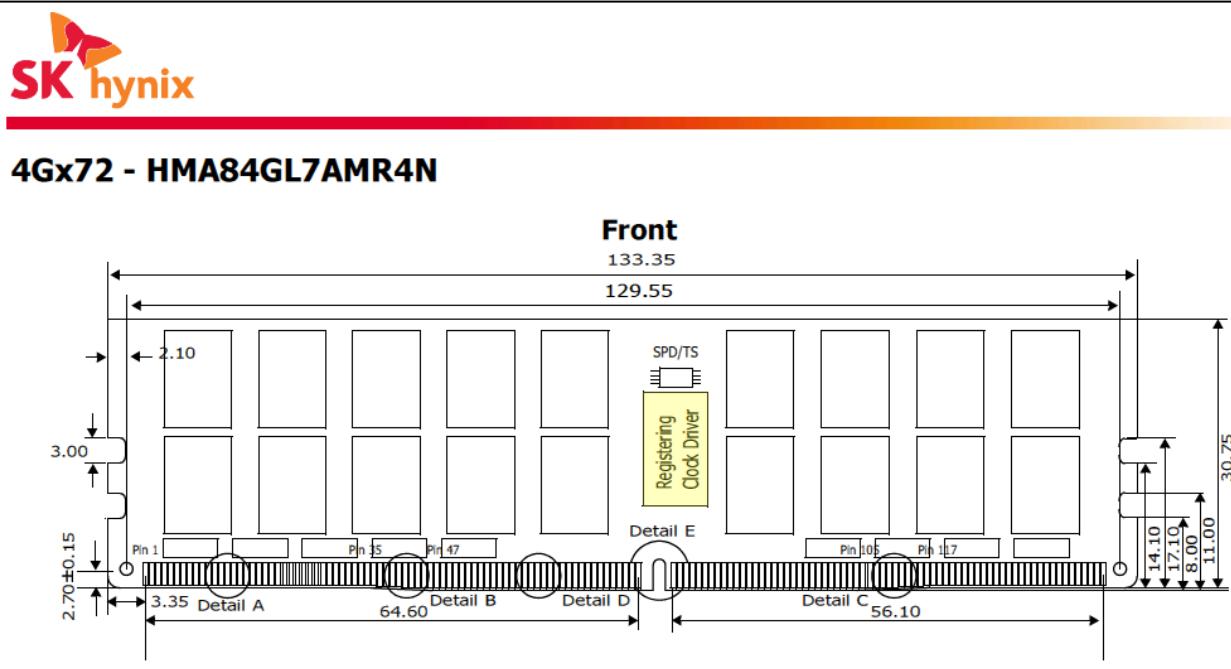
SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 65 (annotations added).

Further, the SK hynix Products include a JEDEC-compliant register clock driver ("RCD") that is accessible by a system memory controller via a system memory bus.

Some modules have lower current requirements. Any specific module must meet the SDRAM, **DDR4RCD01**, and **DDR4DB01** voltage requirements for its worst case supply currents.

See, e.g., JEDEC LRDIMM Specification (annotation added).

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"



SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 65 (annotations added).

Specifically, the SK hynix Products contain an IDT 4RCD0124KC0 RCD.



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).

The IDT 4RCD0124KC0 RCD is JEDEC Compliant.

Features

- JEDEC Compliant RCD

See 4RCD0124K DDR4 Register Clock Driver Webpage at 1.

BENEFITS

- All devices are JEDEC® compliant and meet stringent requirements for reliability and application compliance

IDT Leader in Server Memory Chipsets at 1.

The SK hynix Products further comply with the JEDEC SDRAM Standard, JESD79-4.

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"

**JEDEC
STANDARD**

DDR4 SDRAM

JESD79-4A

(Revision of JESD79-4, September 2012)

JEDEC DDR4 SDRAM Specification (annotations added).

See also SKH DDR4 Device Operation at 1.

The RCD is accessible by a system memory controller via a system memory bus.

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"

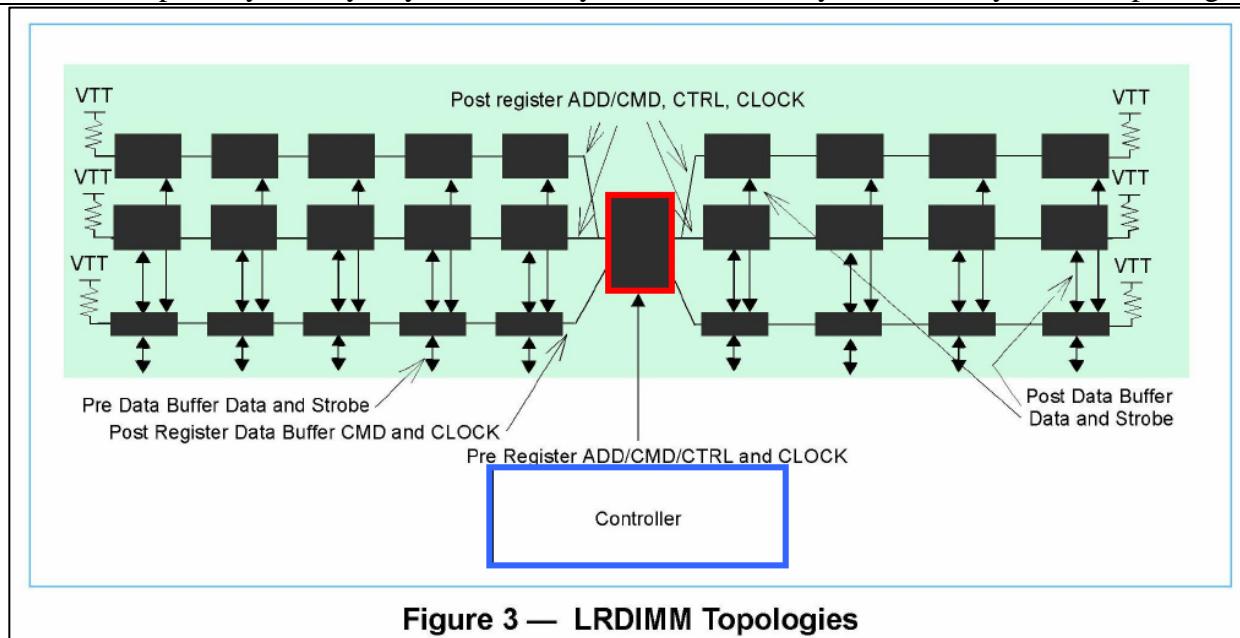


Figure 3 — LRDIMM Topologies

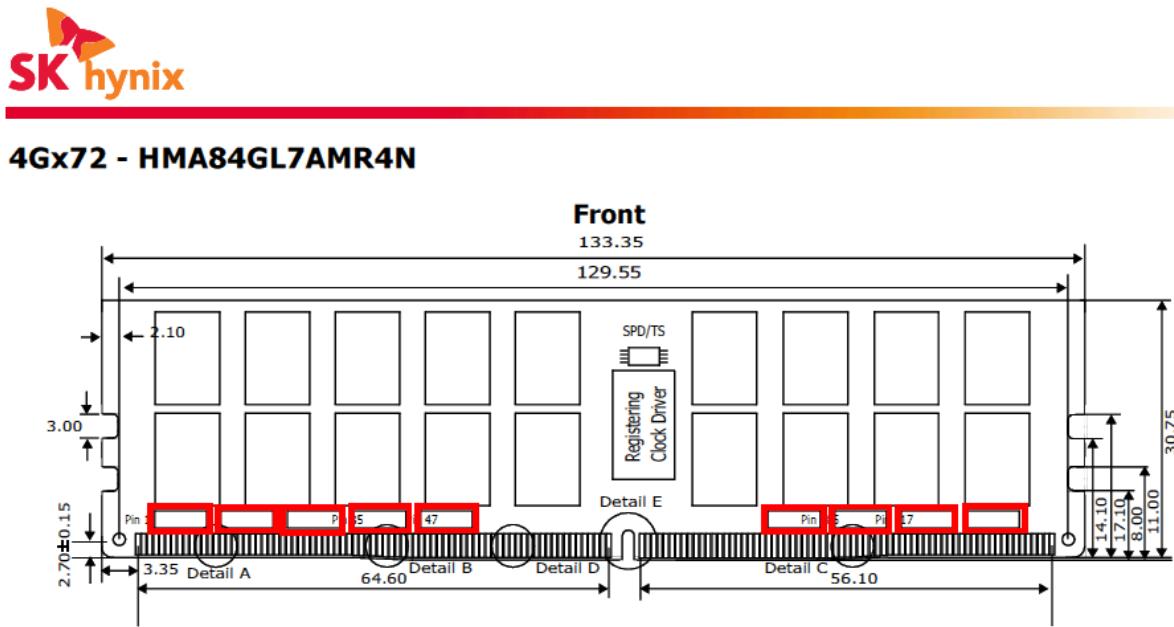
JEDEC LRDIMM Specification (annotations added).

Further, the SK Hynix Products include a plurality of IDT 4DB0226KA3AVG8 Data Buffers. The below picture of the SK Hynix HMA84GL7AMR4N-TFTE AB DIMM is representative of the SK Hynix LRDIMM Products and the data buffers they include.



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-TFTE AB).

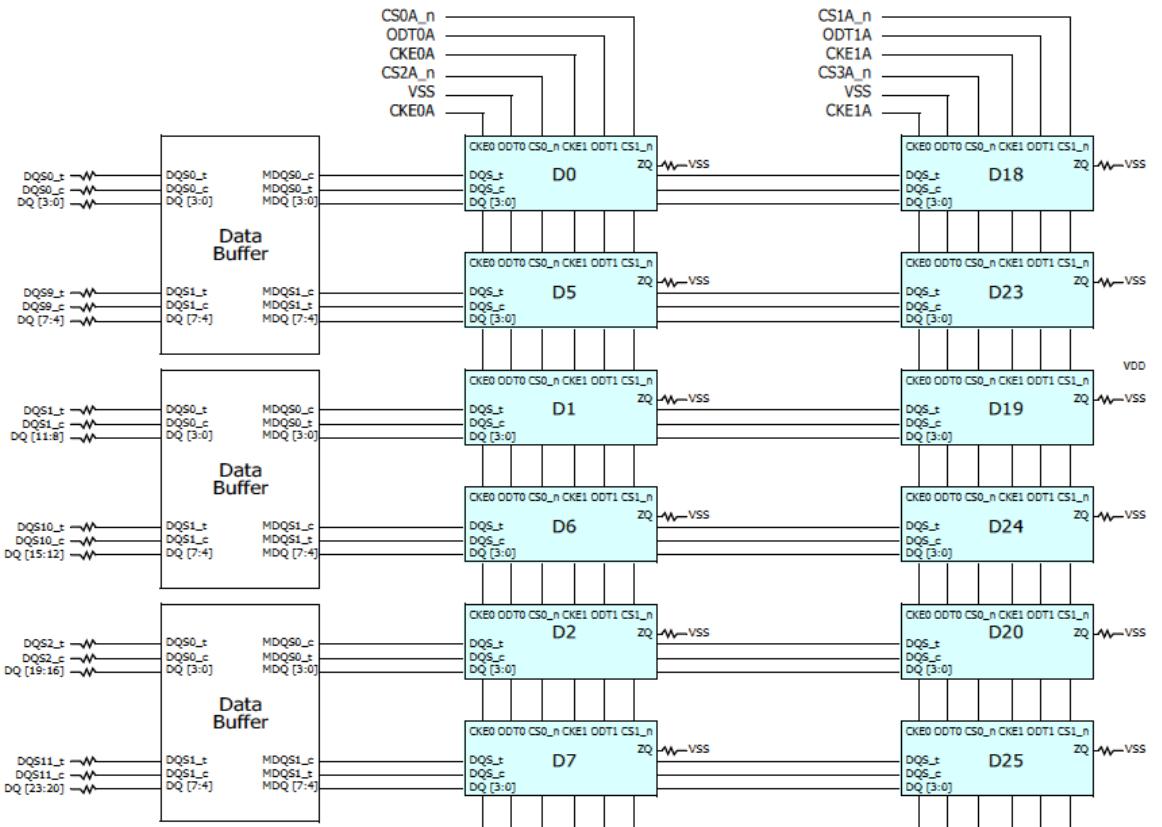
"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"



See HMA84GL7AMR4N Datasheet.

The data buffers are coupled between the data ports of the memory devices and the system memory bus.

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"



See HMA84GL7AMR4N Datasheet

2.1 Description

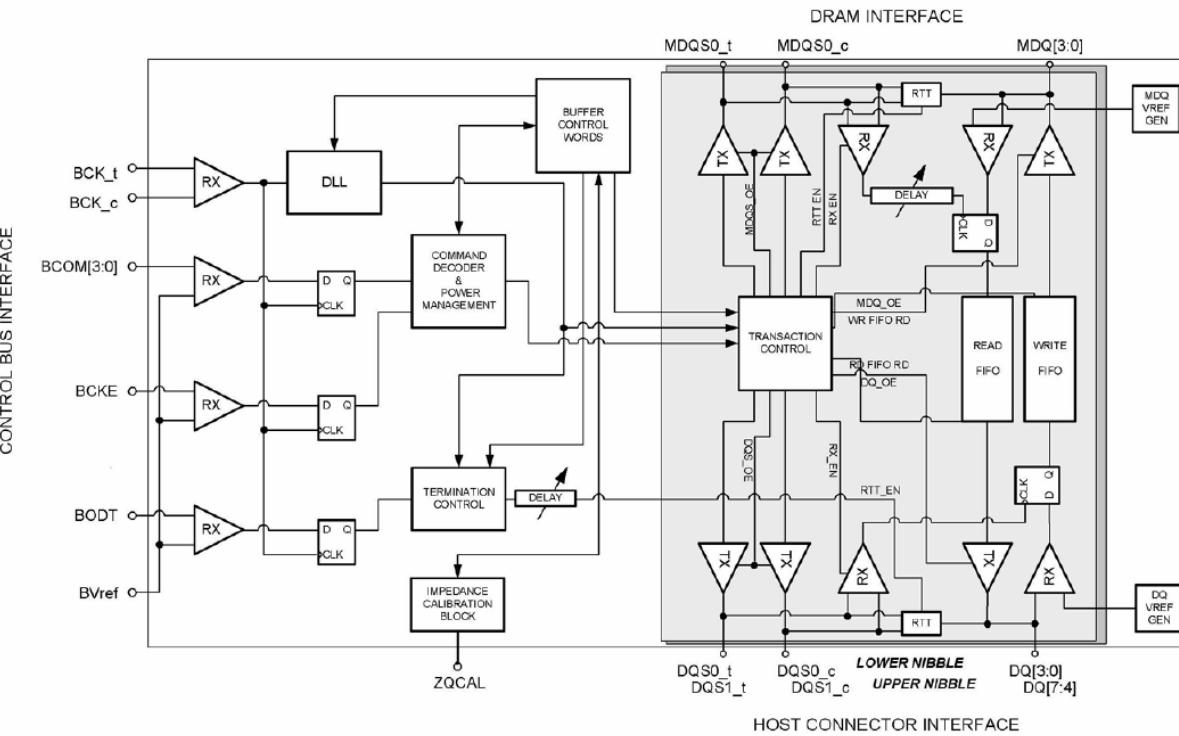
This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V VDD operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

See DDR4DB01 Standard

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"

2.6 Logic Diagram

Figure 12 — Logic Diagram



See DDR4DB01 Standard

"1. A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising:"

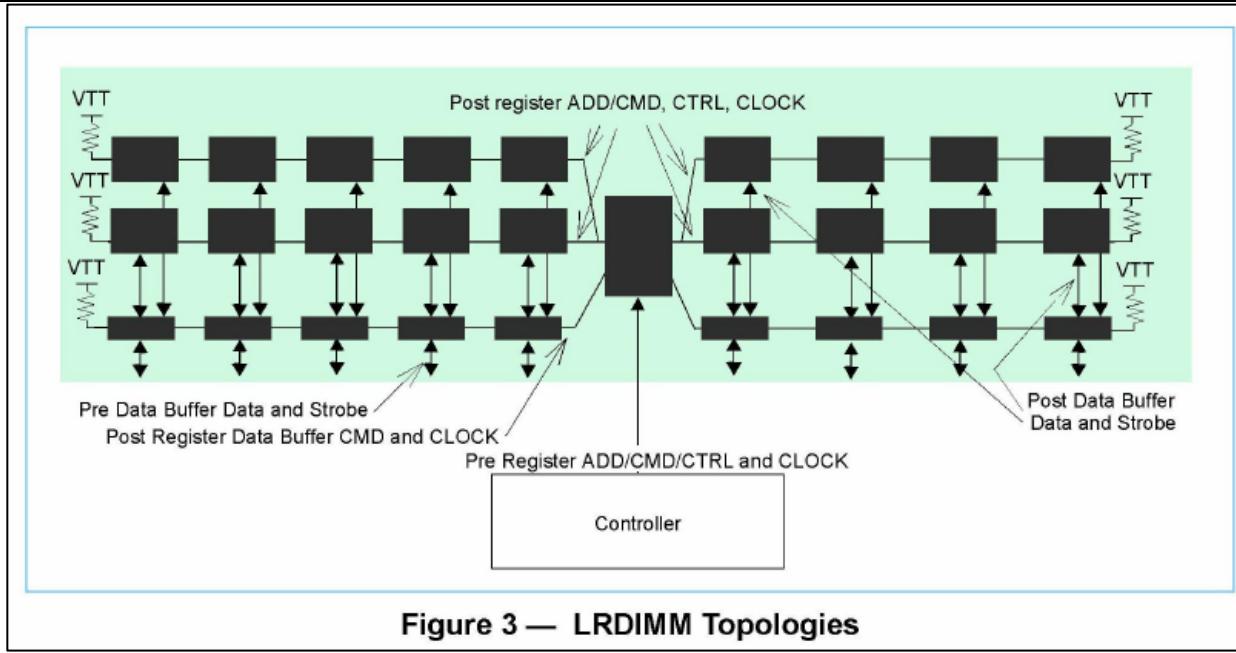


Figure 3 — LRDIMM Topologies

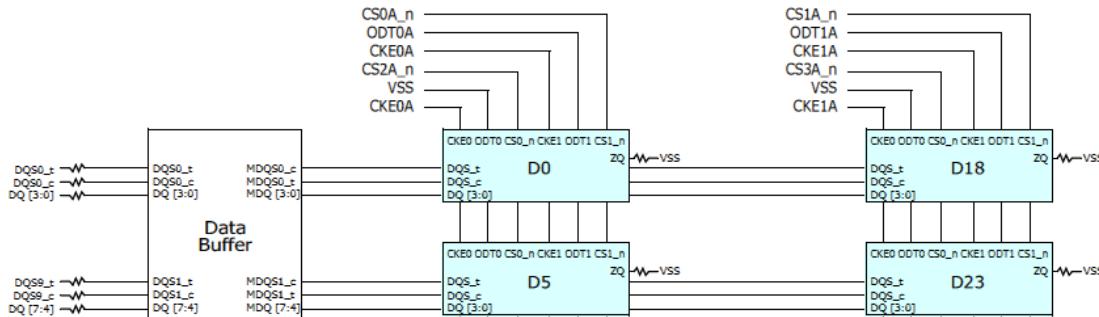
See JEDEC LRDIMM Specification.

"memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;"

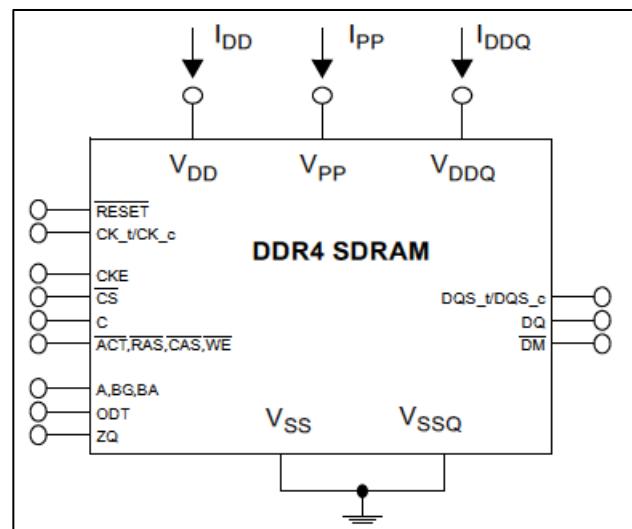
<p>memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;</p>	<p>The SK hynix Products comprise memory devices mounted on a circuit board, the memory devices having address and control ports and data ports.</p> <p>For example, the SK hynix Product includes a plurality of JEDEC-compliant synchronous dynamic random access memories ("SDRAMs") mounted on a circuit board.</p> <div style="border: 1px solid black; padding: 10px;"> <p style="text-align: right;">JEDEC Standard No. 21C Page 4.20.27-5</p> <h2>1 Product Description</h2> <p>This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs. Reference design examples are included that provide an initial basis for DDR4 LRDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666, and PC4-3200 support. All DDR4 LRDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.</p> <p>An additional lower voltage of TBD is defined. PC4L is used to reference DIMMs capable of operation at this voltage level. The annex for each raw card will have specific entries to indicate DIMM operation at PC4 and PC4L voltage levels.</p> <p style="background-color: #ffff00; border: 1px solid black; padding: 2px;">This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org).</p> <p><i>See JEDEC LRDIMM Specification (annotations added).</i></p> </div>
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"memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;"

32GB, 4Gx72 Module(4Rank of x4) - page1



See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 14 (showing SDRAM devices D0, D18, D5, and D23).



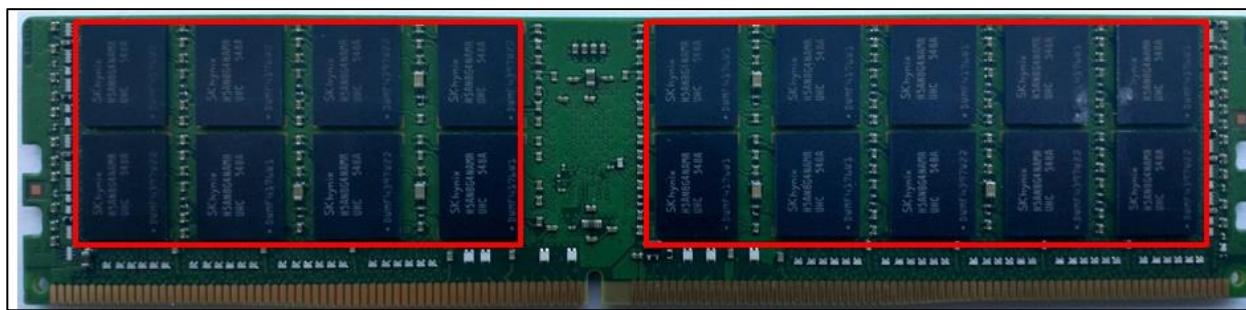
See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 51.

Specifically, the SK hynix HMA84GL7AMR4N-UHTE comprises 36 SDRAM components.

"memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE) (front side).



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE) (back side).



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE) (SDRAM).

The SDRAM devices are JEDEC compliant.

"memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;"

JEDEC STANDARD

DDR4 SDRAM

JESD79-4A

(Revision of JESD79-4, September 2012)

See JEDEC DDR4 SDRAM Specification (annotations added).

See also SKH DDR4 Device Operation at 1.

The SDRAM devices are outlined in red in the figure below.

"memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;"

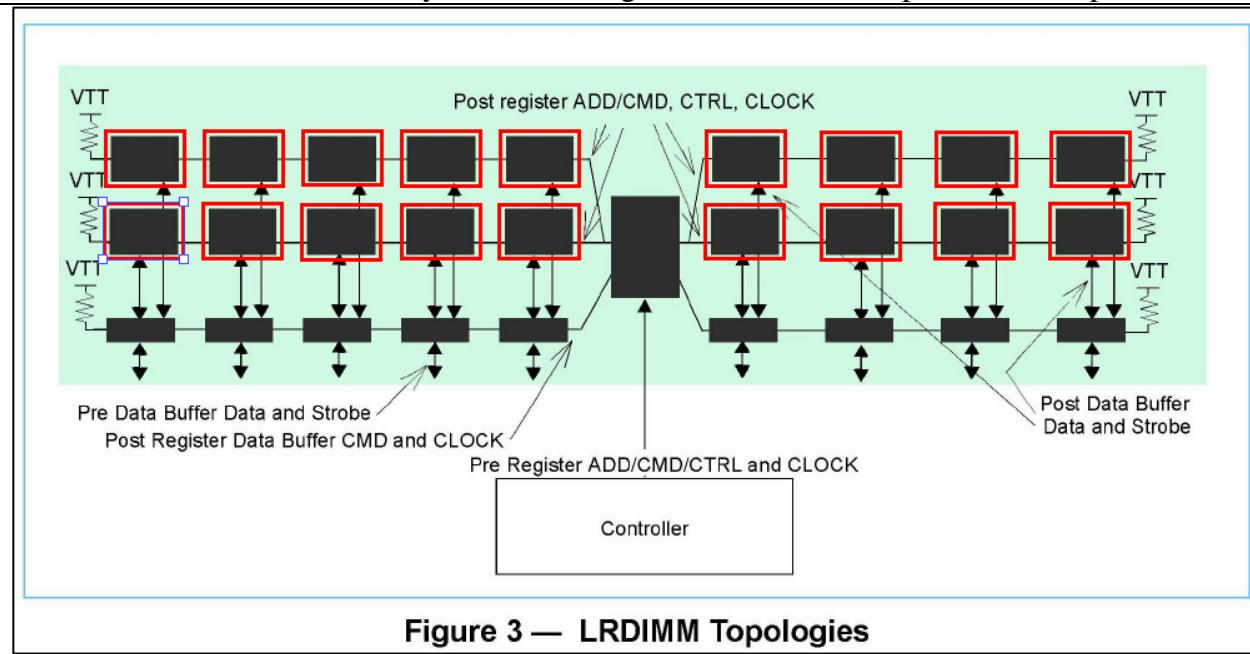


Figure 3 — LRDIMM Topologies

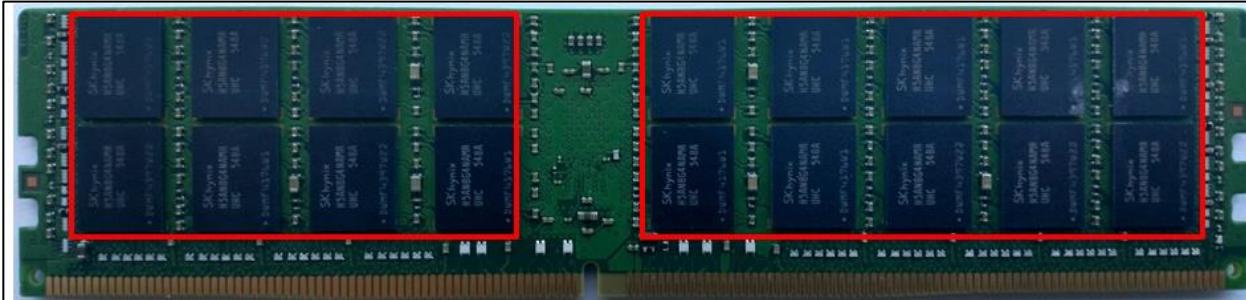
See JEDEC LRDIMM Specification (annotation added).

See also SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 65.



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE) (front side).

"memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE) (back side).

Further, each of the memory devices comprises data, address, and control ports.



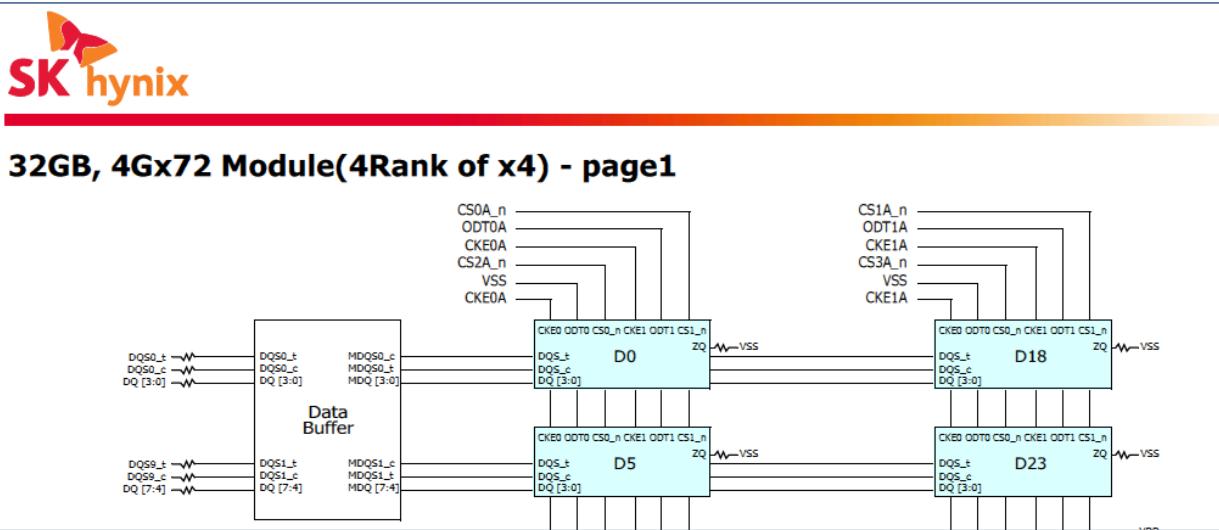
Description

The H5AN8G4NAMR-xxC is a 8Gb CMOS Double Data Rate IV (DDR4) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. SK hynix 8Gb DDR4 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

See SK Hynix 8Gb DDR4 SDRAM (H5AN8G4NAMR-xxC) Technical Data Sheet, Rev. 1.2 (March 2016).

The below images show the control ports (*e.g.*, CS0..., CS1..., CS2..., CS3...), address ports (*e.g.*, A0-A17) and data ports (*e.g.*, DQ, DQS) of each DDR4 SDRAM device (D0, D5, D18, and D23).

"memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;"



See HMA84GL7AMR4N Datasheet (showing DDR4 SDRAM devices D0, D5, D18, and D23 with control ports (e.g., CS0..., CS1..., CS2..., CS3...) and data ports (e.g., DQ, DQS)).

"memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;"



Package Ballout/Mechanical Dimension

x4 Package Ball out (Top view): 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	NC				DM_n, DBI_n	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	NC	DQ2				DQ3	NC	VSSQ	D
E	VSS	VDDQ	NC				NC	VDDQ	VSS	E
F	VDD	ODT1	ODT				CK_t	CK_c	VDD	F
G	VSS	CKE1	CKE				CS_n	CS1_n	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N

See H5AN8G4NAMR-xxC Datasheet (showing data (e.g., DQ, DQS), address (e.g., BA, BG, A...), and control ports (e.g., CS, RAS, CAS, WE)).

DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

See H5AN8G4NAMR-xxC Datasheet.

"memory devices mounted on a circuit board, the memory devices having address and control ports and data ports;"

		<table border="1"> <tr> <td>A0 - A17</td><td>Input</td><td>Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.</td></tr> </table>	A0 - A17	Input	Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.			
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<p><i>See H5AN8G4NAMR-xxC Datasheet.</i></p> <table border="1"> <tr> <td>BG0 - BG1</td><td>Input</td><td>Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Pre-charge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.</td></tr> <tr> <td>BA0 - BA1</td><td>Input</td><td>Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Pre-charge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.</td></tr> </table>			BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Pre-charge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.	BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Pre-charge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
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<p><i>See H5AN8G4NAMR-xxC Datasheet.</i></p> <table border="1"> <tr> <td>CS_n, (CS1_n)</td><td>Input</td><td>Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.</td></tr> </table>			CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.			
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<p><i>See H5AN8G4NAMR-xxC Datasheet.</i></p> <table border="1"> <tr> <td>RAS_n/A16, CAS_n/A15, WE_n/A14</td><td>Input</td><td>Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.</td></tr> </table>			RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.			
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<p><i>See H5AN8G4NAMR-xxC Datasheet.</i></p>								

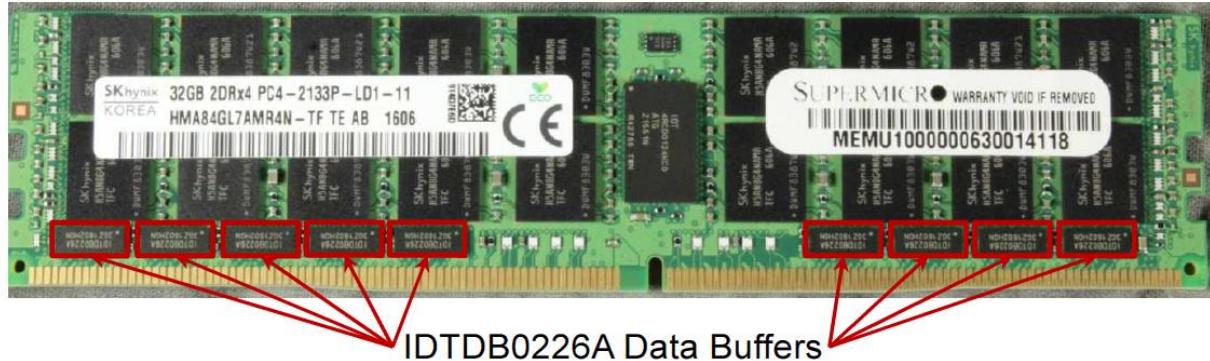
"a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements; and"

a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements; and

The SK hynix Products comprise a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements.

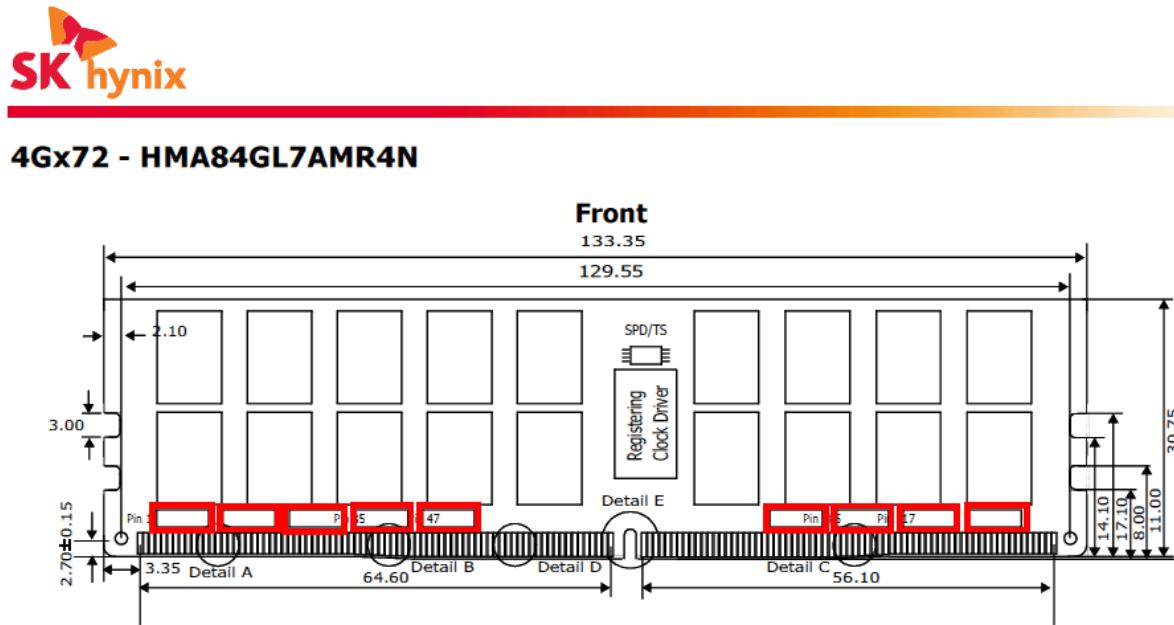
The SK hynix Products include a circuit that comprises a data module mounted on the printed circuit board. For example, the SK Hynix Products include a plurality of IDT 4DB0226KA3AVG8 Data Buffers on its printed circuit board.

The below picture of the SK Hynix HMA84GL7AMR4N-TFTE AB DIMM is representative of the SK Hynix LRDIMM Products and the data buffers they include.



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-TFTE AB).

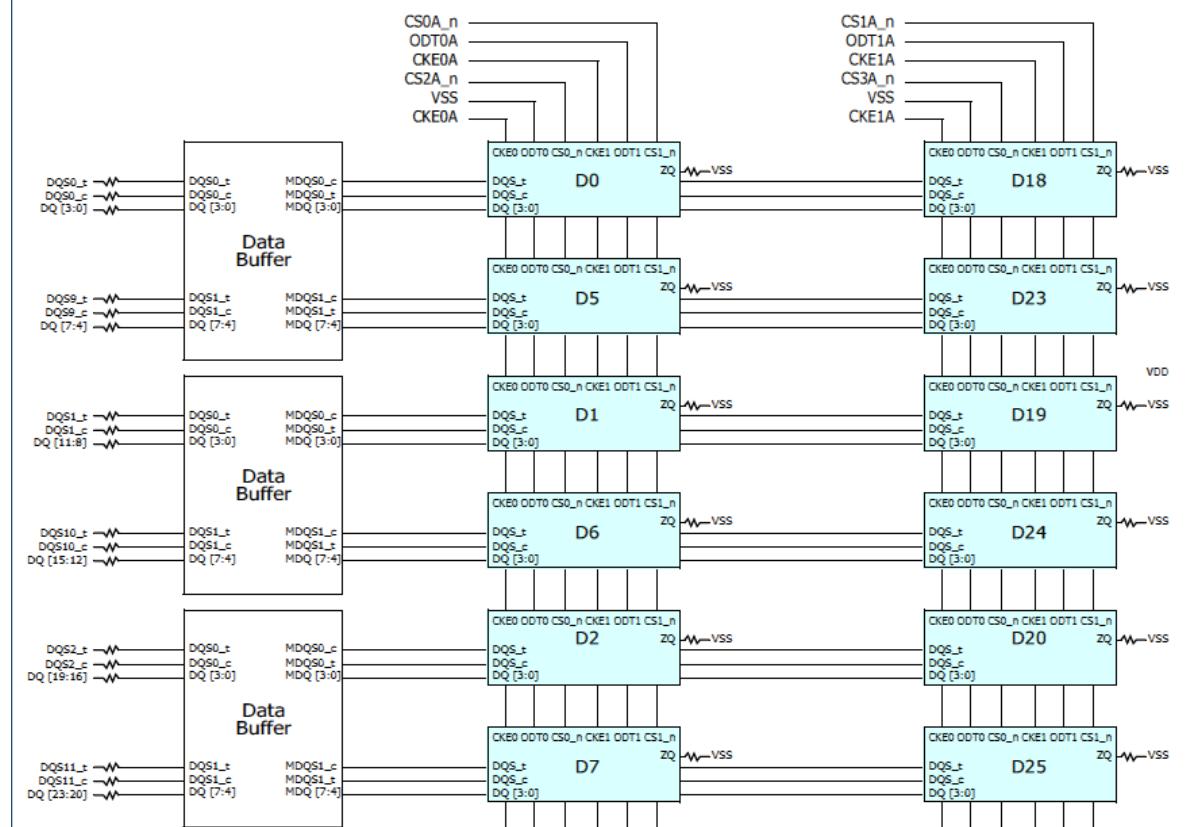
"a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements; and"



See HMA84GL7AMR4N Datasheet.

Further, the data module is coupled between the data ports of the memory devices and the system memory bus. For example, the plurality of data buffers are coupled between corresponding DDR4 SDRAM memory devices and a system memory bus.

"a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements; and"



See HMA84GL7AMR4N Datasheet

2.1 Description

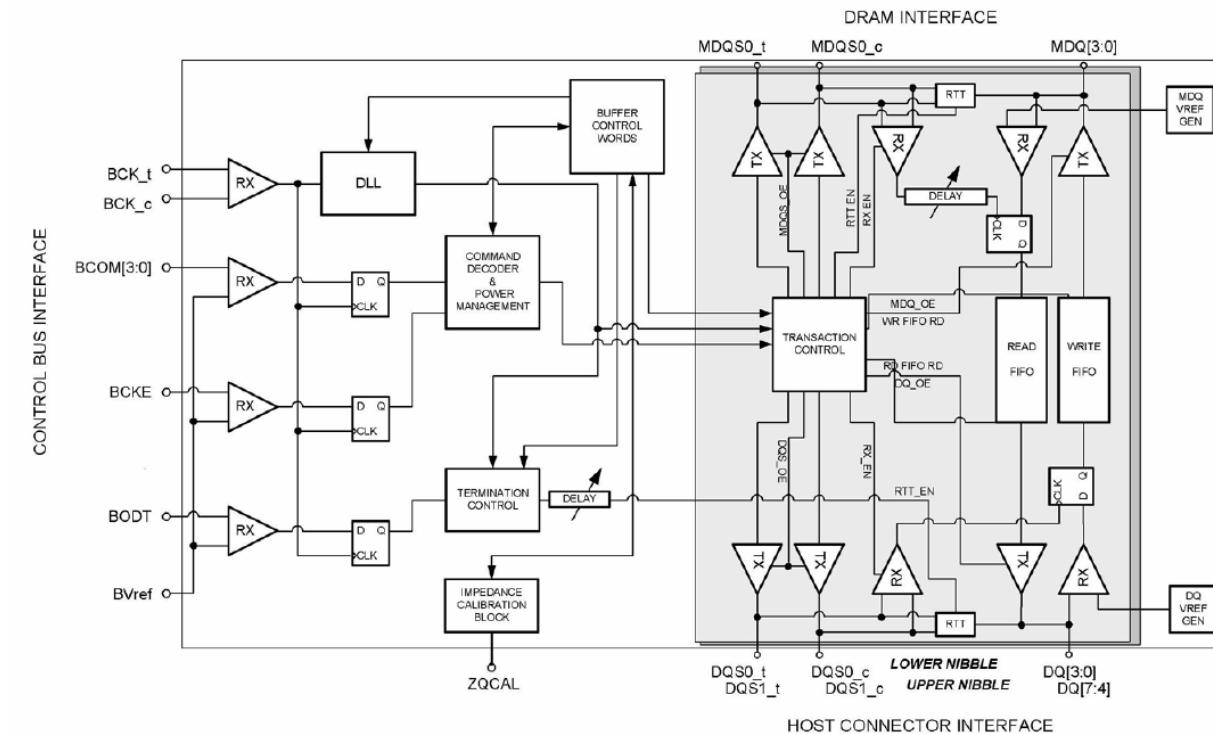
This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V VDD operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

See DDR4DB01 Standard

"a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements; and"

2.6 Logic Diagram

Figure 12 — Logic Diagram



See DDR4DB01 Standard

"a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements; and"

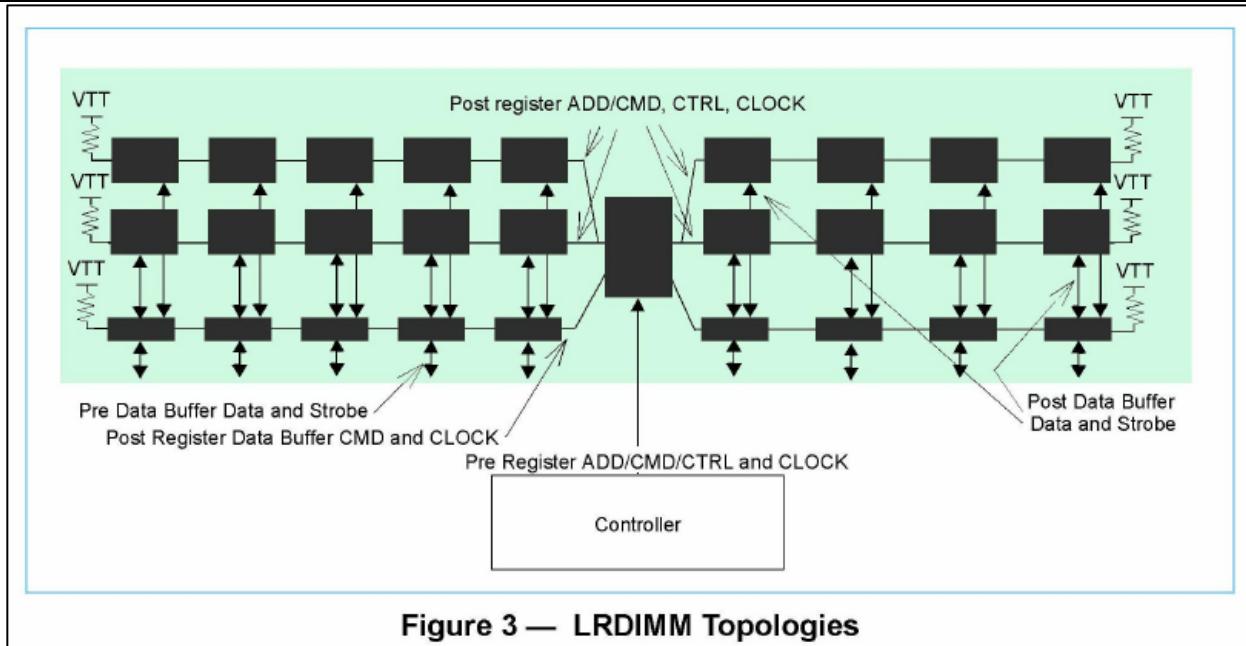


Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification.

Further, each JEDEC compliant IDT Data Buffer includes data handler logic elements, which, among other things, are configured to propagate, transmit and/or provide data patterns to and from the data ports of corresponding memory devices.

2.1 Description

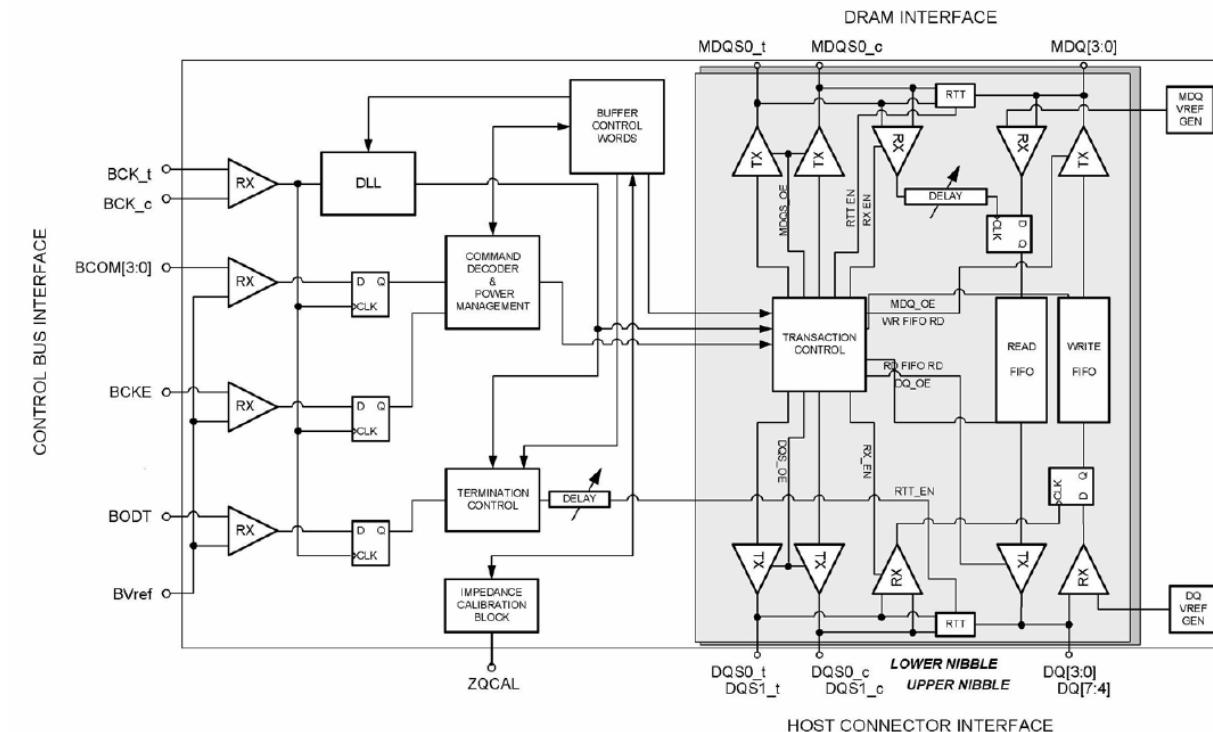
This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V VDD operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

See DDR4DB01 Standard.

"a data module mounted on the circuit board and coupled between the data ports of the memory devices and the system memory bus, the data module including data handler logic elements; and"

2.6 Logic Diagram

Figure 12 — Logic Diagram



See DDR4DB01 Standard.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

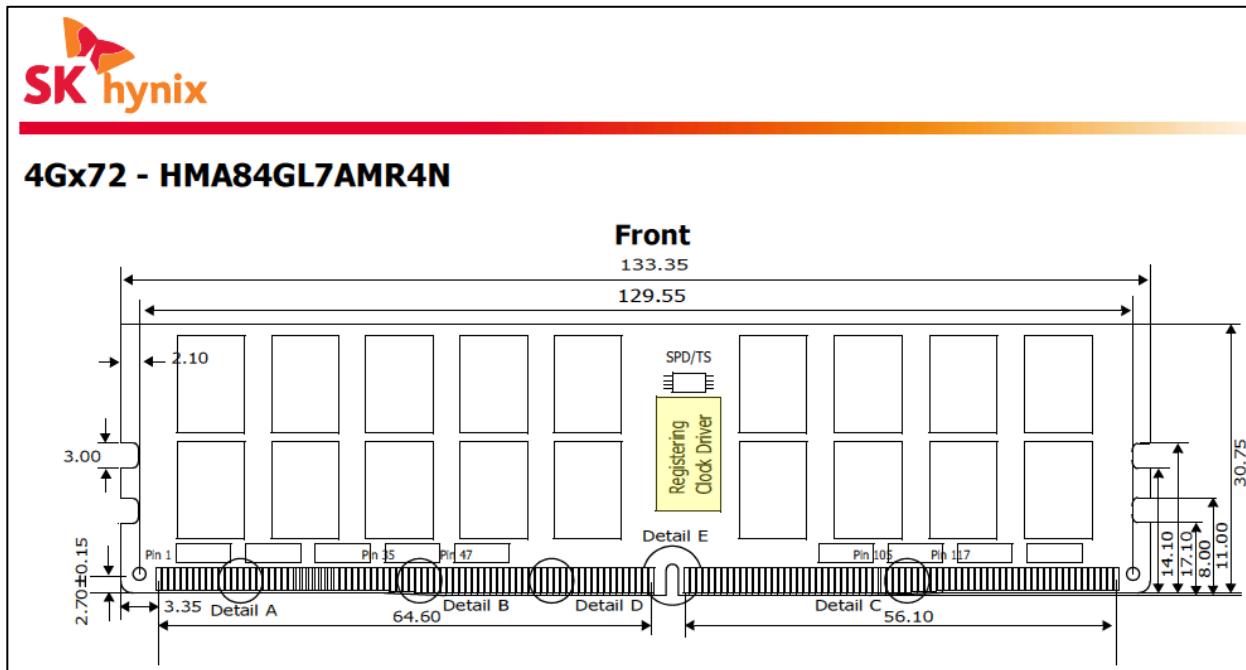
a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and

The SK hynix Products comprise a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus.

The SK hynix Products comprise a control module mounted on the printed circuit board. For example, the SK hynix Products contain a JEDEC-compliant IDT 4RCD0124KC0 RCD on the circuit board.

Some modules have lower current requirements. Any specific module must meet the SDRAM, **DDR4RCD01**, and **DDR4DB01** voltage requirements for its worst case supply currents.

See, e.g., JEDEC LRDIMM Specification (annotation added).



SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 65 (annotations added).

Specifically, the SK hynix Products contain a IDT 4RCD0124KC0 RCD.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).

The IDT 4RCD0124KC0 RCD is JEDEC Compliant.

Features

- JEDEC Compliant RCD

See 4RCD0124K DDR4 Register Clock Driver Webpage at 1.

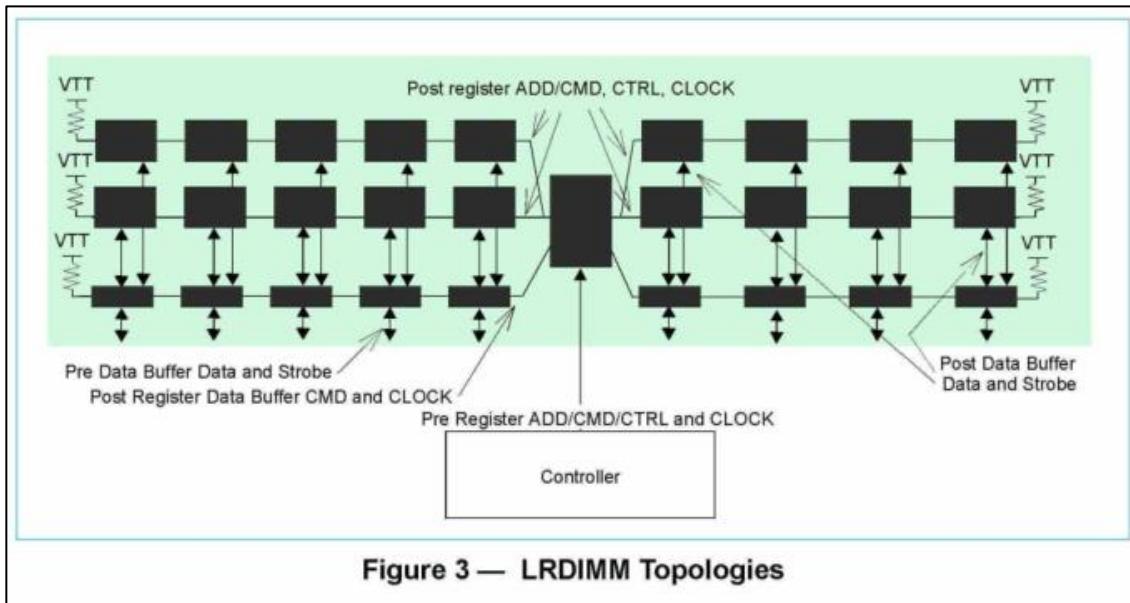
BENEFITS

- All devices are JEDEC® compliant and meet stringent requirements for reliability and application compliance

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

IDT Leader in Server Memory Chipsets at 1.

The SK hynix Products comprise a control module coupled to the data module. For example, the IDT 4RCD0124KC0 RCD is coupled to the IDT data buffers.

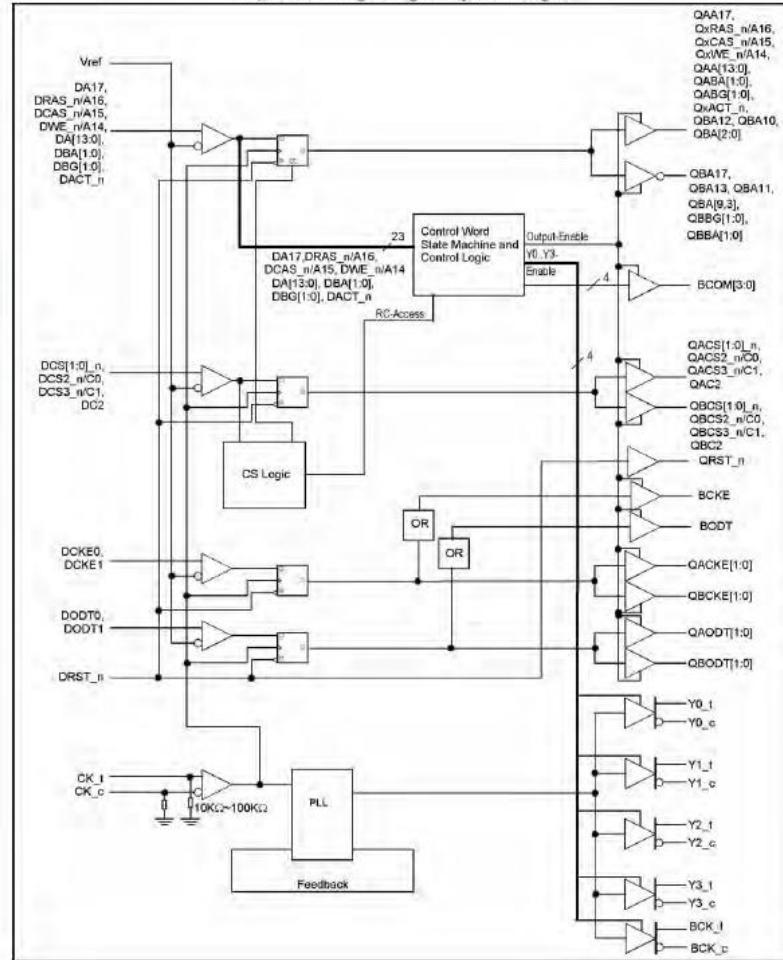


See JEDEC LRDIMM Specification.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



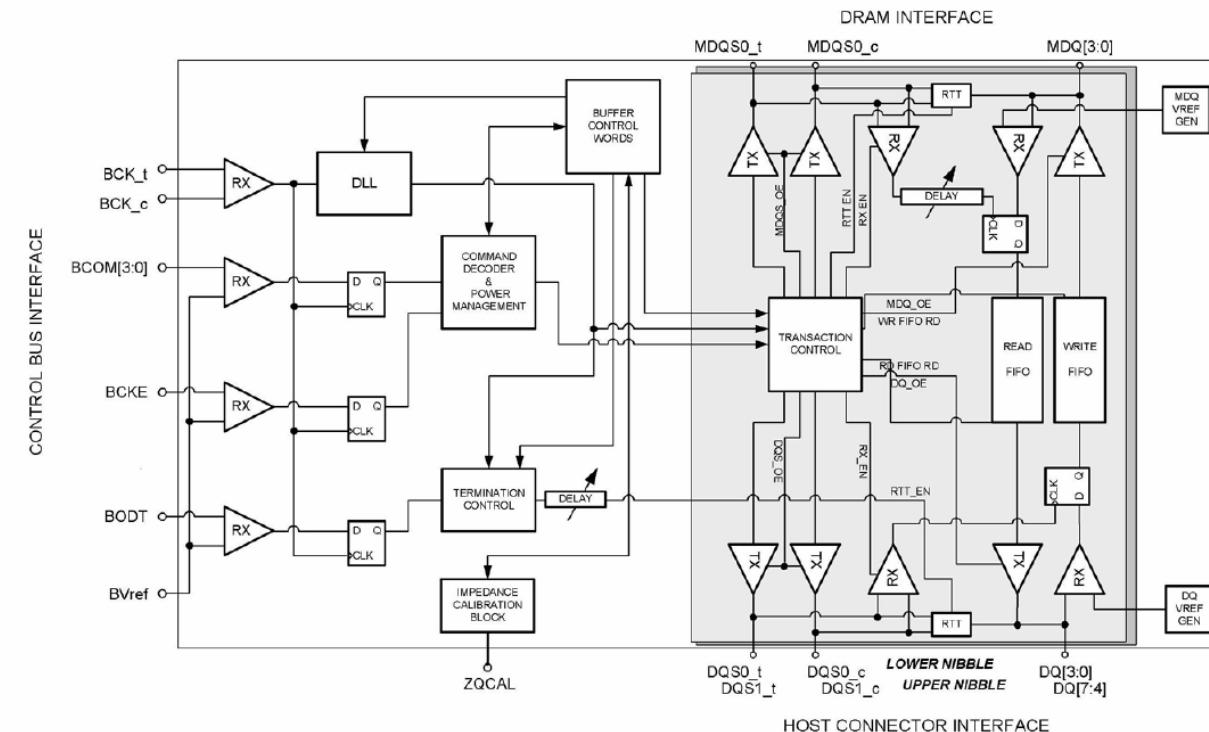
See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

2.6 Logic Diagram

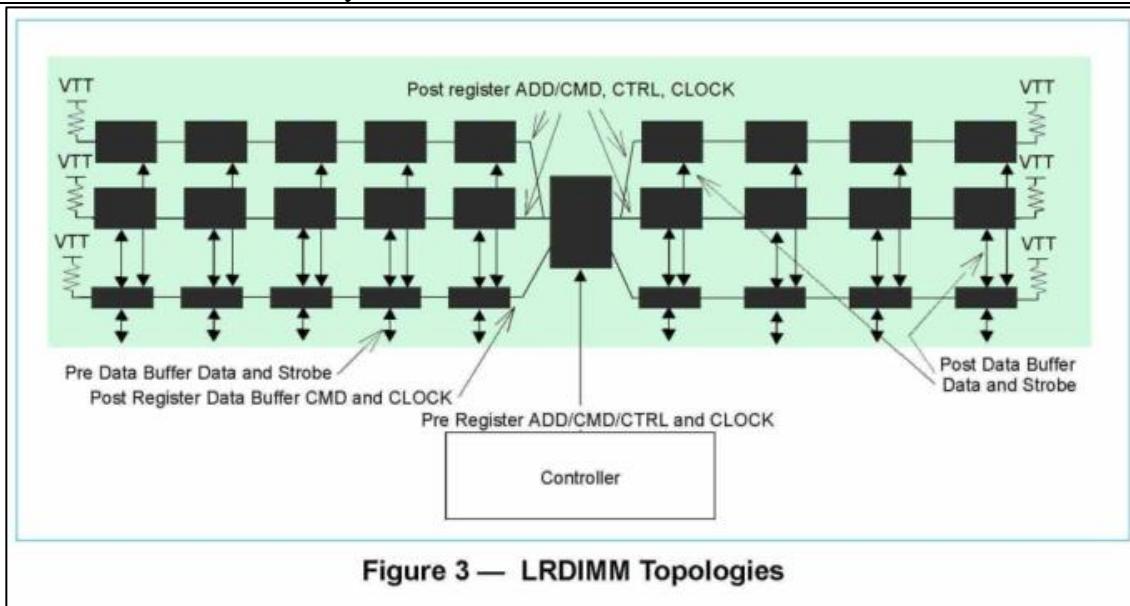
Figure 12 — Logic Diagram



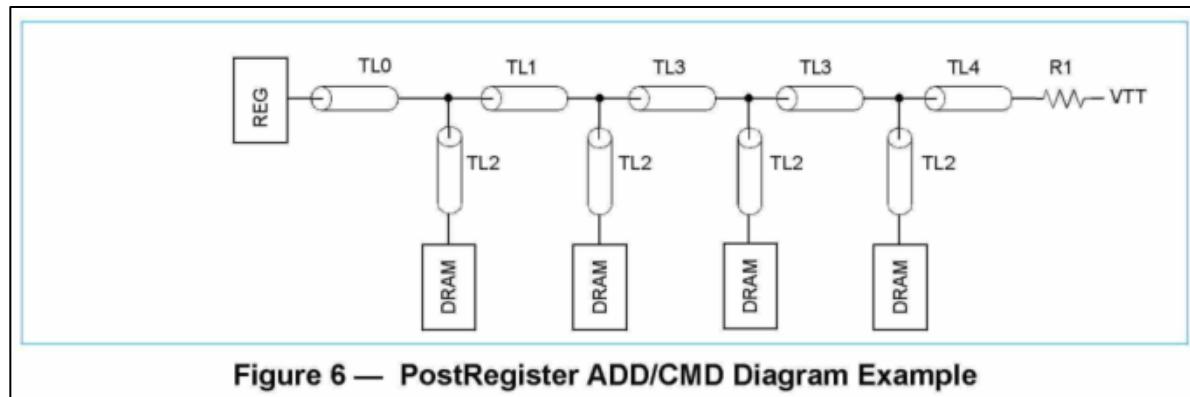
See DDR4DB01 Standard.

The SK hynix Products comprise a control module coupled to the address and control ports memory devices. For example, the IDT 4RCD0124KC0 RCD is coupled to the address and control ports of the plurality of dynamic random access memory elements on the PCB.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"



JEDEC LRDIMM Specification.

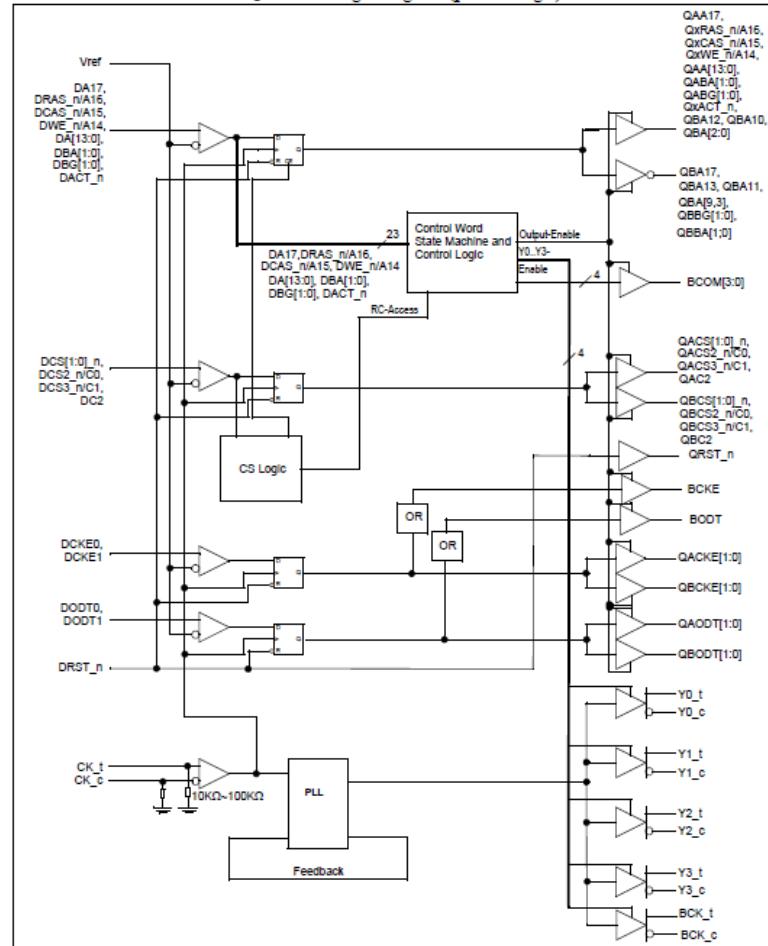


JEDEC LRDIMM Specification.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n	CMOS ¹ V _{REF} based	Some of these have alternative functions: <ul style="list-style-type: none"> DCS2_n <=> DC0 DCS3_n <=> DC1
Input Address and Command bus	DC0..DC1	CMOS ¹ V _{REF} based	
	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal.
	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
Clock inputs	DA14..DA16	CMOS ¹ V _{REF} based	In case of an ACT command some of these terminals have an alternative function:
	DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	DRAM corresponding register command signals. <ul style="list-style-type: none"> DA14 <=> DWE_n DA15 <=> DCAS_n DA16 <=> DRAS_n
	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
Clock inputs	CK_LCK_c	CMOS differential	Differential master clock input pair to the PLL, with a 10KΩ~100KΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

Table 16 — Terminal functions

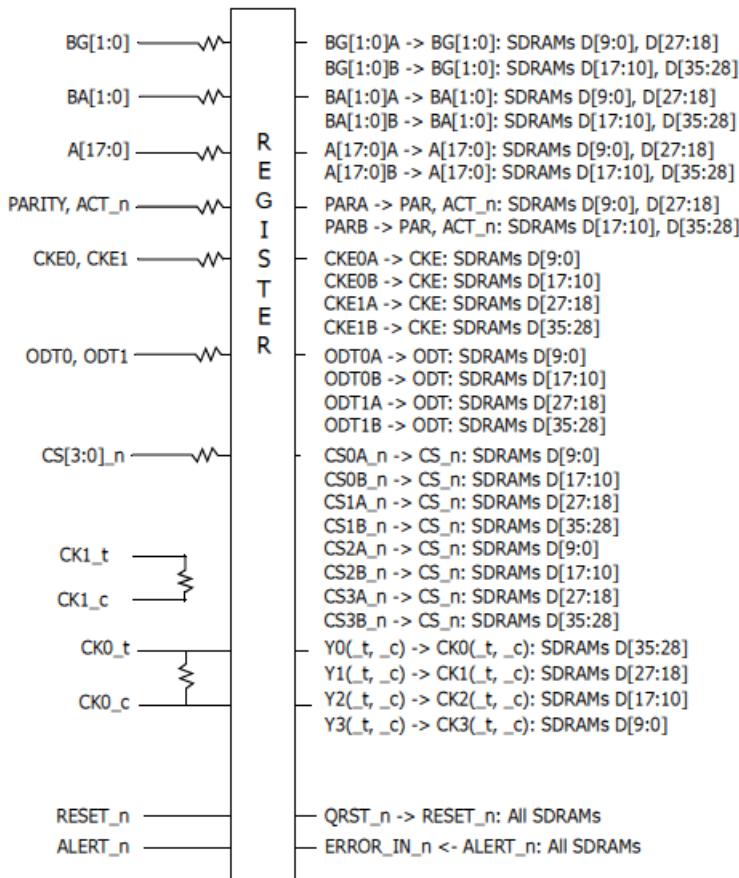
Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS ²	Register output CKE and ODT signals.
	QACS0_n, QACSI_n, QBCS0_n, QBCSI_n	CMOS ²	Register output Chip Select signals.
	QACS2_n, QACSI_n, QBCS2_n, QBCSI_n or QAC0..QAC1, QBC0..QBC1	CMOS ²	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACI_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	VrefCA	V _{DD} ²	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"



32GB, 4Gx72 Module(4Rank of x4) - page3

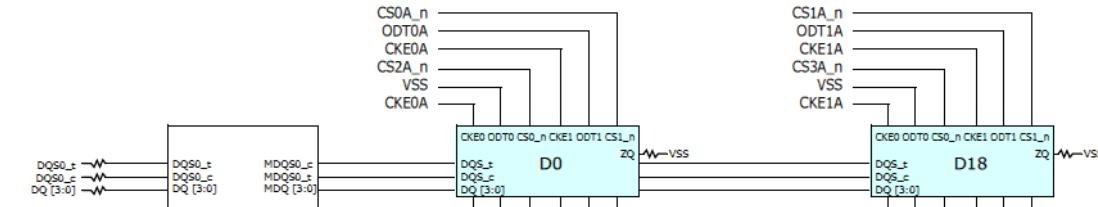


SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 16.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"



32GB, 4Gx72 Module(4Rank of x4) - page1



SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 14.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid]

Table 16 — Command Truth Table

Function	Abbrevi- ation	CKE		CS_n	ACT_n	RAS_n	CAS_n	WE_n	A14	BG0- BG1	BA0- BA1	C2-C0	A12/ BC_n	A17/ A15	A18/ AP	Ad-AS	NOTE
		Pre- Cycle	Current Cycle														
Mode Register Set	MRS	H	H	L	H	L	L	L		BG	BA	V			OP Code	12	
Refresh	REF	H	H	L	H	L	L	H		V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H		V	V	V	V	V	V	V	
Self Refresh Exit	SRX	L	H	H	X	X	X	X		X	X	X	X	X	X	X	
Single Bank Precharge	PRE	H	H	L	H	L	H	L		BG	BA	V	V	V	V	L	
Precharge all Banks	PREA	H	H	L	H	L	H	L		V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H							RFU		
Bank Activate	ACT	H	H	L	L				Row Address (RA)		BG	BA	V		Row Address (RA)		
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L		BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L		BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L		BG	BA	V	H	V	L	CA	
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L		BG	BA	V	V	V	H	CA	
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L		BG	BA	V	L	V	H	CA	
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L		BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H		BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H		BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDSS	H	H	L	H	H	L	H		BG	BA	V	H	V	L	CA	
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H		BG	BA	V	V	V	H	CA	
Read with Auto Pre-charge (BL8, on the Fly)	RDAS4	H	H	L	H	H	L	H		BG	BA	V	L	V	H	CA	
Read with Auto Pre-charge (BC4, on the Fly)	RDAS8	H	H	L	H	H	L	H		BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H		V	V	V	V	V	V	V	
Device Deselected	DES	H	H	H	X	X	X	X		X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X		X	X	X	X	X	X	6	
Power Down Exit	PDX	L	H	H	X	X	X	X		X	X	X	X	X	X	X	
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L		V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L		V	V	V	V	V	L	V	

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t_NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set Commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQLO-DQL7; DQSU corresponds to the data on DQ0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DB/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
NOTE: Input only pins (BG0-BG1,BA0-BA1,A0-A17,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT, and RESET_n) do not supply termination.		

See JEDEC DDR4 DRAM Specification.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"



Package Ballout/Mechanical Dimension

x4 Package Ball out (Top view): 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	NC				DM_n, DBI_n	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	NC	DQ2				DQ3	NC	VSSQ	D
E	VSS	VDDQ	NC				NC	VDDQ	VSS	E
F	VDD	ODT1	ODT				CK_t	CK_c	VDD	F
G	VSS	CKE1	CKE				CS_n	CS1_n	TEN	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

See H5AN8G4NAMR-xxC Datasheet (showing data (e.g., DQ, DQS), address (e.g., BA, BG, A...), and control ports (e.g., CS, RAS, CAS, WE)).

DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQL_t, DQL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For x16, DQL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQSU0-DQSU7. The data strobe DQS_t, DQL_t, and DQSU_t are paired with differential signals DQS_c, DQL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

See H5AN8G4NAMR-xxC Datasheet.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

A0 - A17	Input	Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
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See H5AN8G4NAMR-xxC Datasheet.

BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Pre-charge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Pre-charge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.

See H5AN8G4NAMR-xxC Datasheet.

CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
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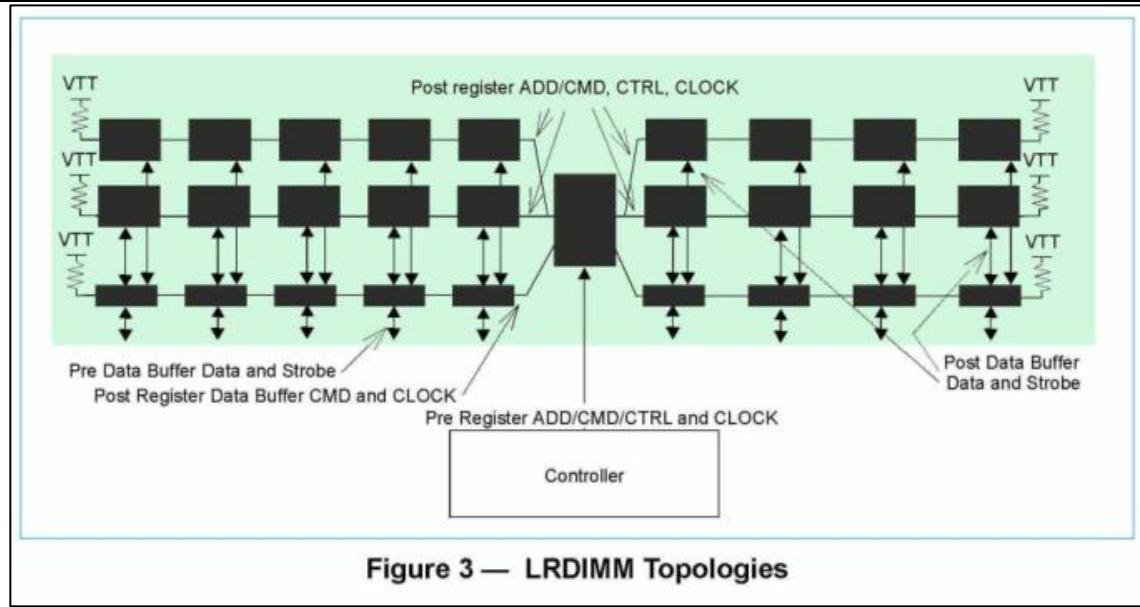
See H5AN8G4NAMR-xxC Datasheet.

RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.
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See H5AN8G4NAMR-xxC Datasheet.

Further, the SK hynix Products include a control module coupled to system memory bus.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

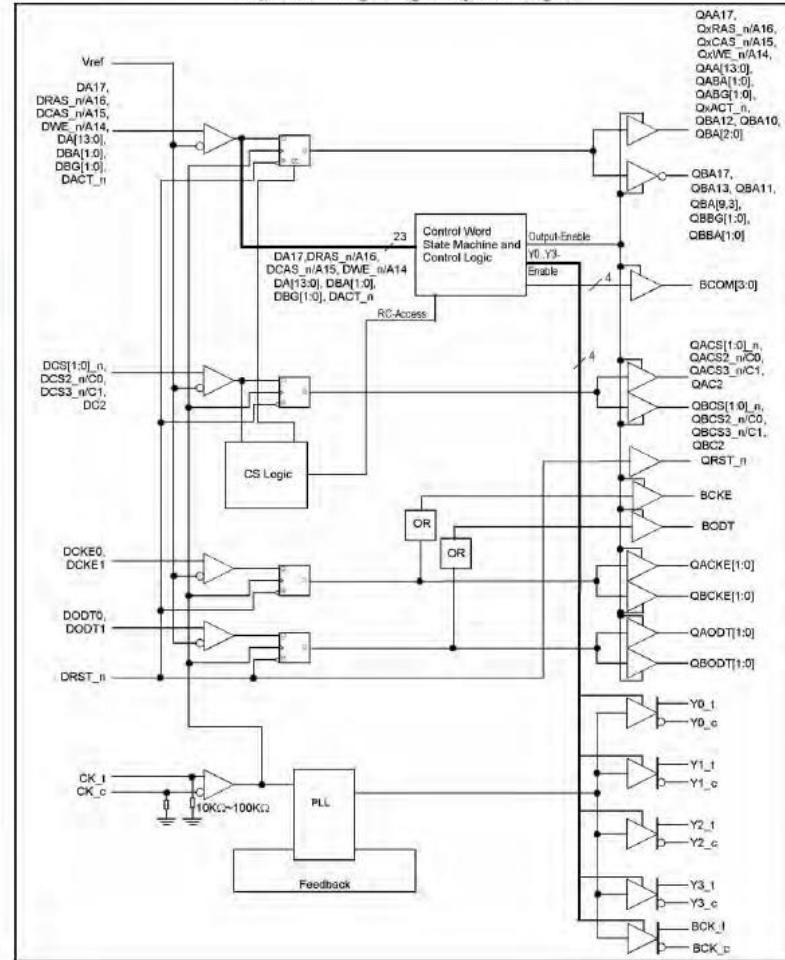


See JEDEC LRDIMM Specification.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"

2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



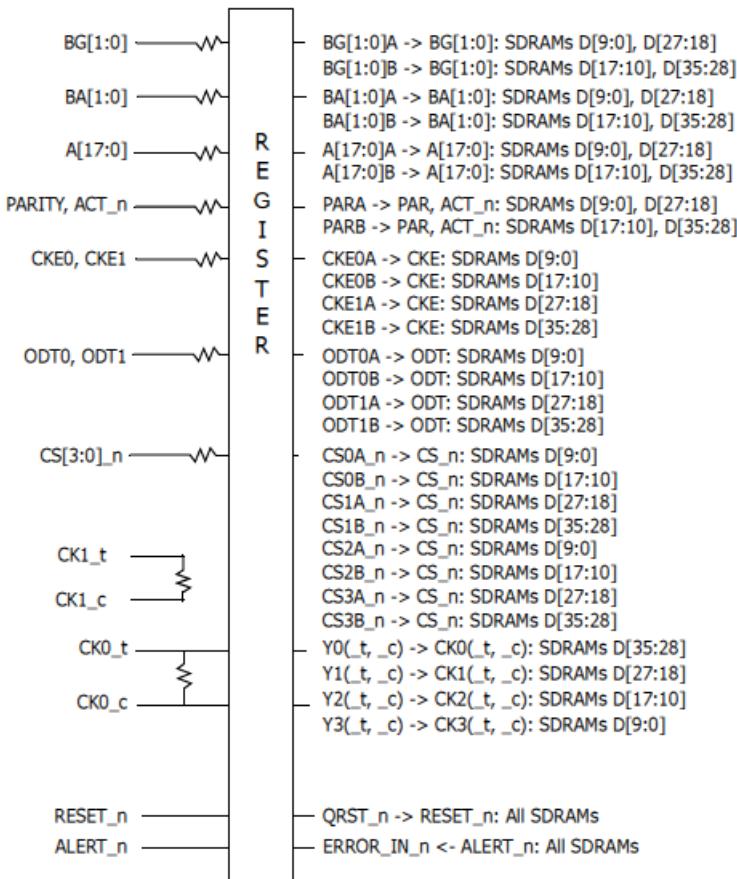
See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"a control module mounted on the circuit board and coupled to the data module, the address and control ports of the memory devices, and the system memory bus; and"



32GB, 4Gx72 Module(4Rank of x4) - page3



See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 16.

"wherein the memory module is operable in any of a plurality of modes including a first mode and a second mode;"

<p>wherein the memory module is operable in any of a plurality of modes including a first mode and a second mode;</p>	<p>The SK hynix Products comprise memory modules wherein the memory module is operable in any of a plurality of modes including a first mode and a second mode.</p> <p>For example, the SK hynix Products are operable in a first mode, e.g., a normal operating mode.</p> <table border="1"> <caption>Table 35 — RC0C: Training Control Word</caption> <thead> <tr> <th>Setting (DA[3:0])</th><th>Definition</th><th>Encoding</th></tr> </thead> <tbody> <tr> <td>x 0 0 0</td><td>Training mode selection</td><td>Normal operating mode</td></tr> <tr> <td>x 0 0 1</td><td></td><td>Clock-to-CA training mode¹</td></tr> <tr> <td>x 0 1 0</td><td></td><td>DCS0_n loopback mode¹</td></tr> <tr> <td>x 0 1 1</td><td></td><td>DCS1_n loopback mode¹</td></tr> <tr> <td>x 1 0 0</td><td></td><td>DCKE0 loopback mode¹</td></tr> <tr> <td>x 1 0 1</td><td></td><td>DCKE1 loopback mode¹</td></tr> <tr> <td>x 1 1 0</td><td></td><td>DODT0 loopback mode¹</td></tr> <tr> <td>x 1 1 1</td><td></td><td>DODT1 loopback mode¹</td></tr> <tr> <td>0 x x x</td><td>Reserved</td><td>Reserved</td></tr> <tr> <td>1 x x x</td><td></td><td>Reserved</td></tr> </tbody> </table> <p>1. In these training modes the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals).</p> <p>See JEDEC RCD01 Specification (annotations added).</p> <p>Further, the SK hynix Products are operable in a second mode, e.g., DB-to-DRAM Write Delay ("MWD") Training Mode.</p>	Setting (DA[3:0])	Definition	Encoding	x 0 0 0	Training mode selection	Normal operating mode	x 0 0 1		Clock-to-CA training mode ¹	x 0 1 0		DCS0_n loopback mode ¹	x 0 1 1		DCS1_n loopback mode ¹	x 1 0 0		DCKE0 loopback mode ¹	x 1 0 1		DCKE1 loopback mode ¹	x 1 1 0		DODT0 loopback mode ¹	x 1 1 1		DODT1 loopback mode ¹	0 x x x	Reserved	Reserved	1 x x x		Reserved
Setting (DA[3:0])	Definition	Encoding																																
x 0 0 0	Training mode selection	Normal operating mode																																
x 0 0 1		Clock-to-CA training mode ¹																																
x 0 1 0		DCS0_n loopback mode ¹																																
x 0 1 1		DCS1_n loopback mode ¹																																
x 1 0 0		DCKE0 loopback mode ¹																																
x 1 0 1		DCKE1 loopback mode ¹																																
x 1 1 0		DODT0 loopback mode ¹																																
x 1 1 1		DODT1 loopback mode ¹																																
0 x x x	Reserved	Reserved																																
1 x x x		Reserved																																

"wherein the memory module is operable in any of a plurality of modes including a first mode and a second mode;"

2.1.8.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.

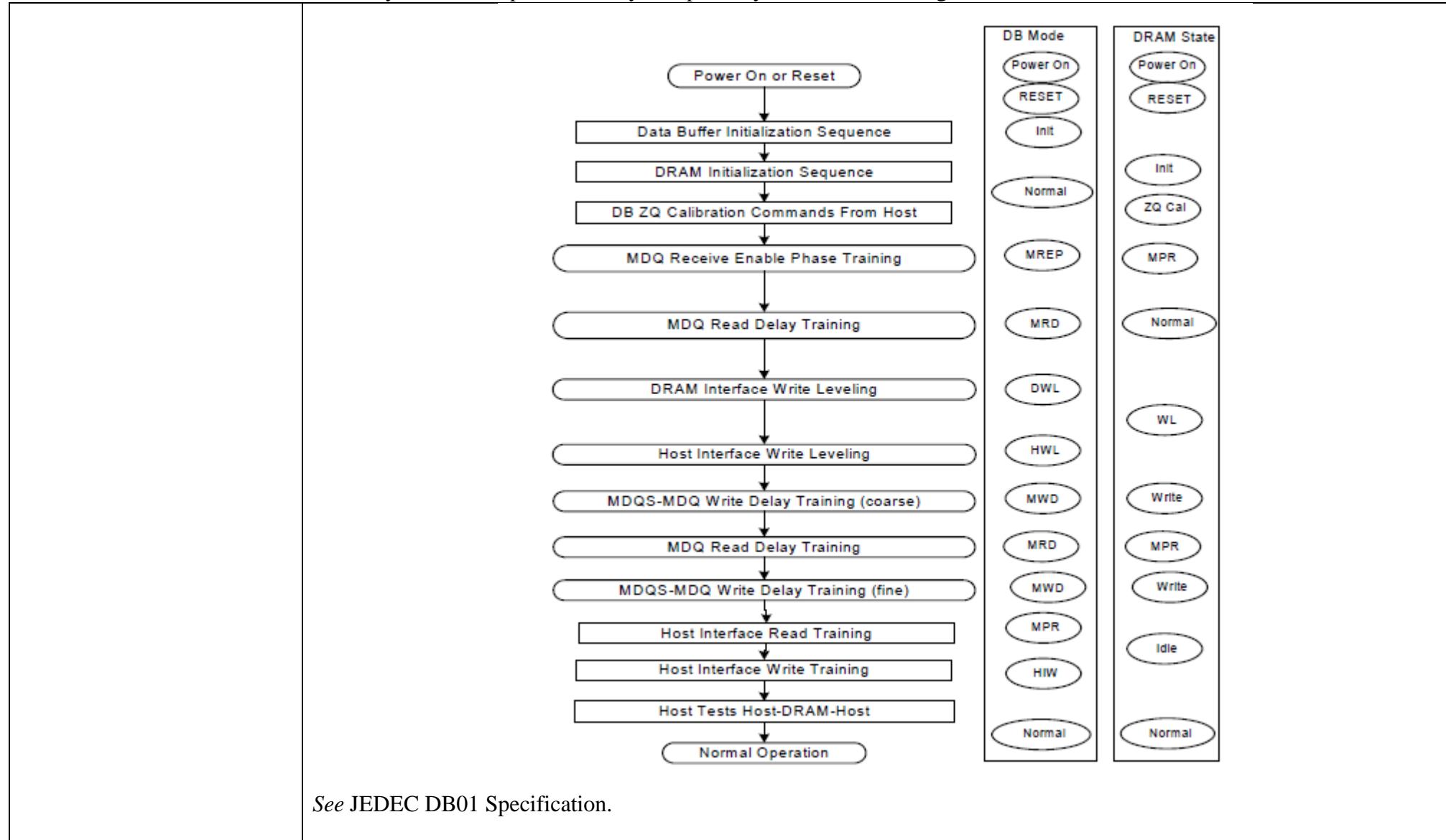
For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3 * 1/64 * t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

See JEDEC DB01 Specification.

The MWD Training Mode is different than normal mode.

"wherein the memory module is operable in any of a plurality of modes including a first mode and a second mode;"



"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

<p>wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and</p>	<p>The SK hynix Products include a control module wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals.</p> <p>The SK hynix products include a control module that, in the first mode, is configured to receive system address and control signals from the system memory controller.</p> <p>(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE)</p> <p>For example, the IDT RCD is configured to receive a set of input address and control signals corresponding to a memory read or write command information (e.g., CS, A0-A17, ACT, RAS, CAS, WE, CKE, etc.) from the memory controller.</p>
--	--

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

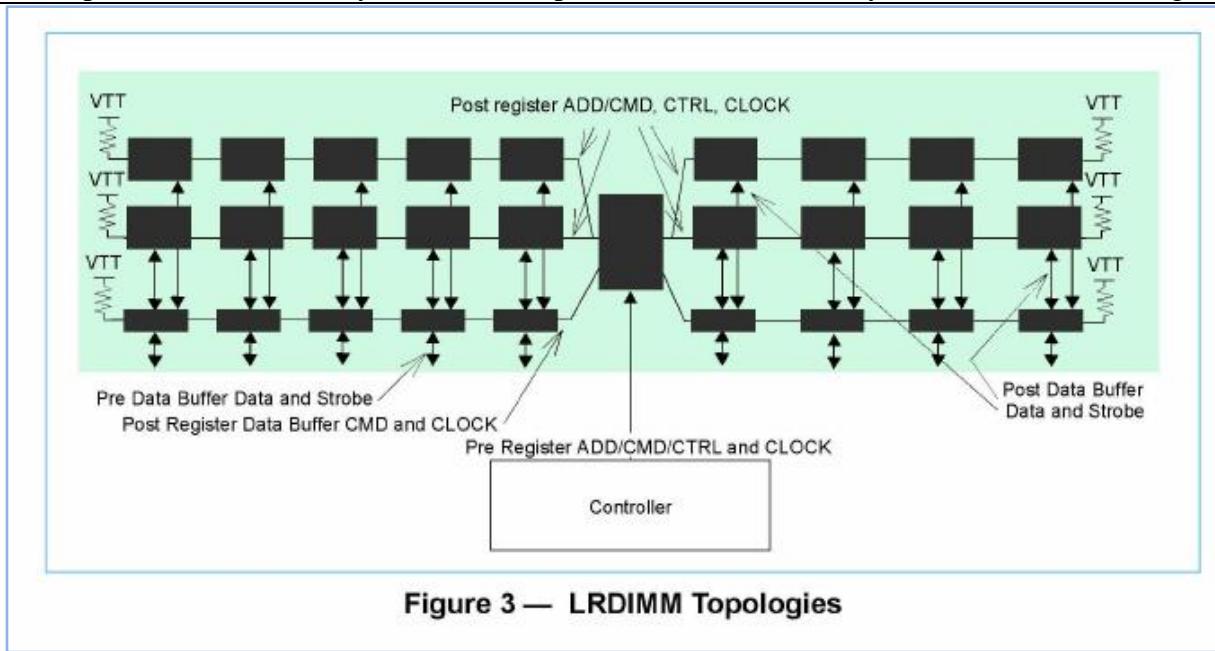


Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification.

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into seven groups. Figure 3 summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. The signal groups are:

1. DQ and DQS signals connector to Data Buffer (DB)
2. DQ and DQS signals DB to SDRAM
3. PreRegister ADD/CMD and CTRL
4. PreRegister CK
5. PostRegister ADD/CMD
6. PostRegister Control
7. PostRegister CK
8. PostRegister BCOM, BODT, BCKE
9. PostRegister BCK

The PreRegister ADD/CMD and CTRL group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, PARITY, CSx_n, CKEx, and ODTx.

The PostRegister ADD/CMD group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, and PARITY.

The PostRegister CTRL group includes CSx_n, CKEx, and ODTx.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

See JEDEC LRDIMM Specification.

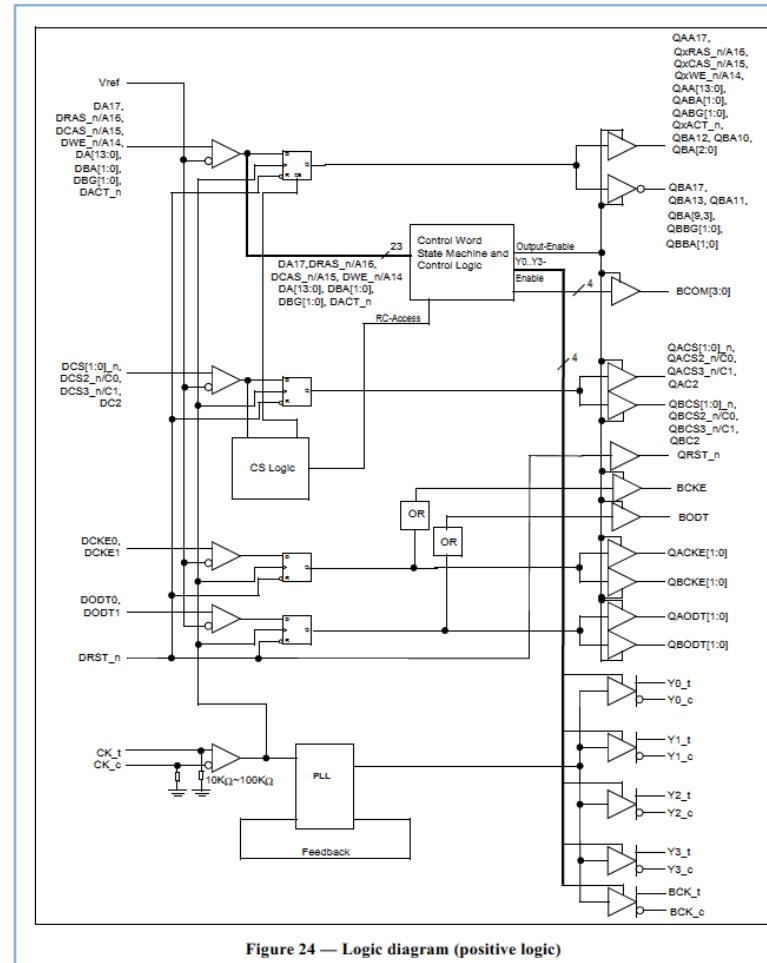
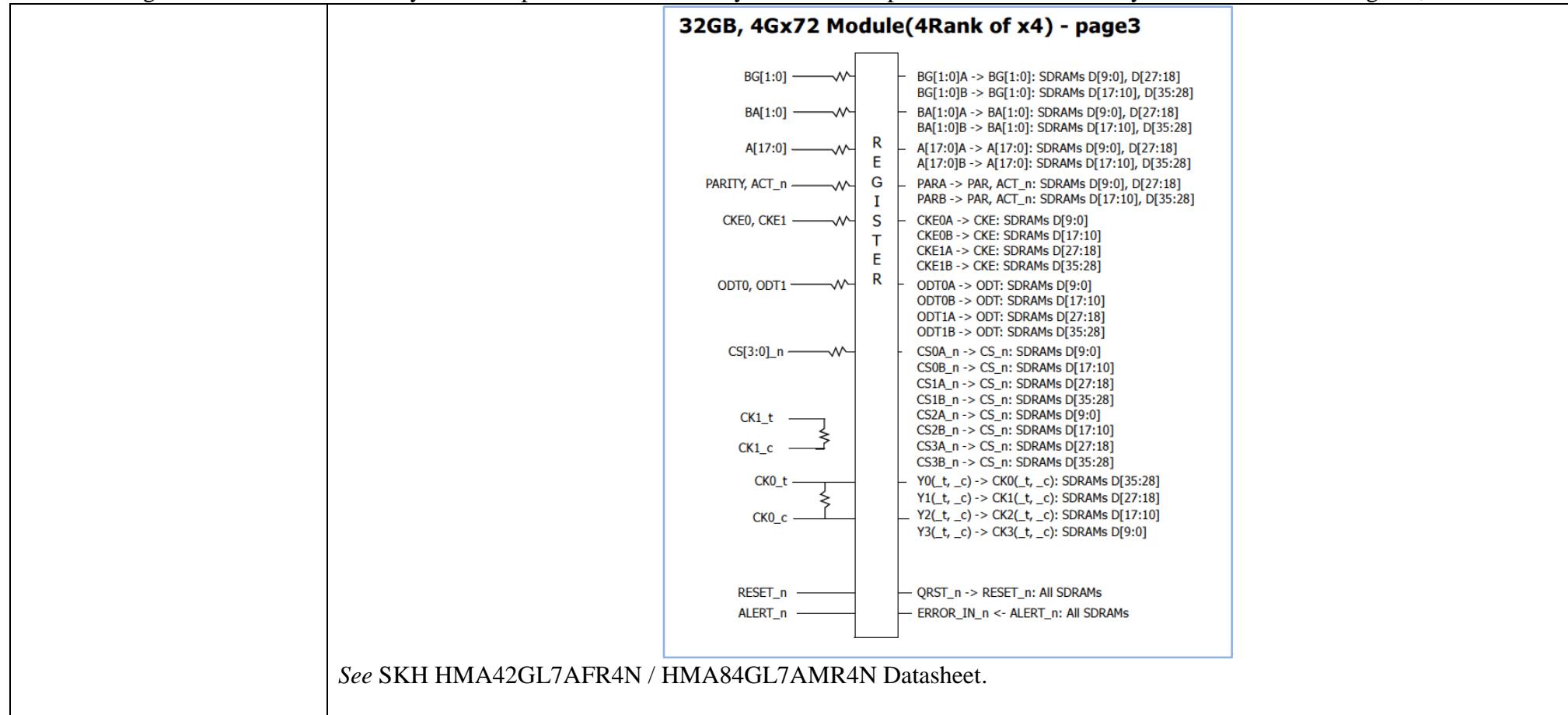


Figure 24 — Logic diagram (positive logic)

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"



"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

Table 4 — Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge, Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT, and CKE, are disabled during power-down. Input buffer, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. These pins are multi-function. For example, for activation with ACT_n Low, the pins are Addresses A16, A15, and A14, but for non-activation commands with ACT_n High, these are Command pins for Read, Write, and other commands defined in the command truth table
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped). See command truth table for details.

See JEDEC LRDIMM Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

4 DDR4 SDRAM Command Description and Operation																
4.1 Command Truth Table																
(a) Note 1,2,3 and 4 apply to the entire Command truth table																
(b) Note 5 applies to all Read/Write commands.																
[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].																
Table 16 — Command Truth Table																
Function	Abbreviation	CKE Pervious Cycle	Current Cycle	CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n /A14	BG0- BG1	BA0- BA1	C2-C8	A12/ BC_n	A17/ A13, A11	A10/ AP	A0-A9	NOTE
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V			OP Code		12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	V
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	V	L	V
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	V	H	V
RFU	RFU	H	H	L	H	L	H	H							RFU	
Bank Activate	ACT	H	H	L	L				Row Address (RA)		BG	BA	V		Row Address (RA)	
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	V	L	CA
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	V	L	CA
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	V	H	CA
Read with Auto Pre-charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Pre-charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	L	V	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	H	V	V	V	V	V	L	V	

NOTE 4: A command is defined as a state where a bit is set or reset. A bit is valid only when it is asserted or deasserted. The last bit of a command is valid only when it is asserted. The first bit of a command is valid only when it is deasserted.

See JEDEC DDR4 DRAM Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n or DC0..DC1	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
Input Address and Command bus	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal.
	DA0..DA13, DAI7	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
Clock inputs	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
	CK_tCK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Reset input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_tBCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
Data buffer control and communication outputs	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

See JEDEC RCD01 Specification.

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/I, QAODT0/I, QBCKE0/I, QBODT0/I	CMOS ²	Register output CKE and ODT signals.
	QACS0_n, QACSI_n, QBCS0_n, QBCSI_n	CMOS ²	Register output Chip Select signals.
	QACS2_n, QACSI_n, QBCS2_n, QBCSI_n	CMOS ²	Register output Chip Select signals. These pins initiate DRAM address/command decodes.
	QAC0..QAC1, QBC0..QBC1	CMOS ²	Some of these have alternative functions: • QnCS2_n <=> QnC0 • QnCS3_n <=> QnC1
Output Address and Command bus	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QnA14 <=> QnWE_n • QnA15 <=> QnCAS_n • QnA16 <=> QnRAS_n
	QAACT_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers
Clock outputs	Y0_t, Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input

See JEDEC RCD01 Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

The SK hynix Products include a control module that is configured to output first memory address and control signals to the memory devices according to the system address and control signals. For example, the IDT RCD outputs memory address and control signals (e.g., as part of read and write commands) to the memory devices according to the system address and control signals.

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into seven groups. Figure 3 summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. The signal groups are:

1. DQ and DQS signals connector to Data Buffer (DB)
2. DQ and DQS signals DB to SDRAM
3. PreRegister ADD/CMD and CTRL
4. PreRegister CK
5. PostRegister ADD/CMD
6. PostRegister Control
7. PostRegister CK
8. PostRegister BCOM, BODT, BCKE
9. PostRegister BCK

The PreRegister ADD/CMD and CTRL group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, PARITY, CSx_n, CKEx, and ODTx.

The PostRegister ADD/CMD group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, and PARITY.

The PostRegister CTRL group includes CSx_n, CKEx, and ODTx.

See JEDEC LRDIMM Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

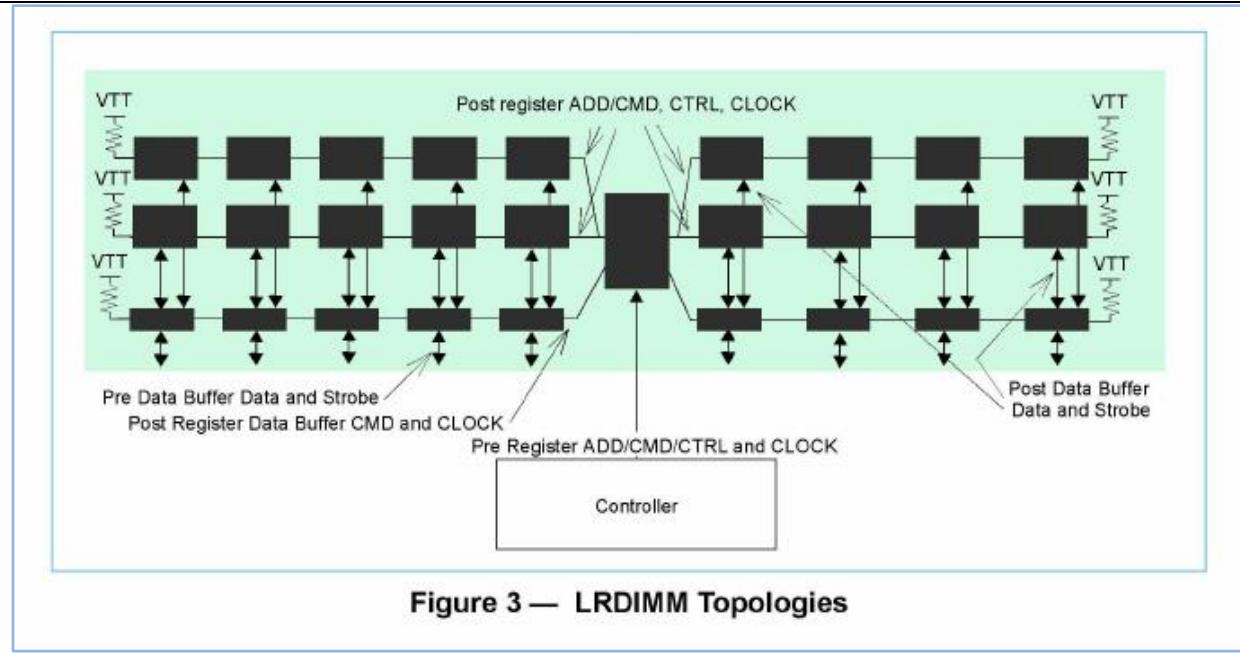


Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

Table 4 — Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge, Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT, and CKE, are disabled during power-down. Input buffer, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. These pins are multi-function. For example, for activation with ACT_n Low, the pins are Addresses A16, A15, and A14, but for non-activation commands with ACT_n High, these are Command pins for Read, Write, and other commands defined in the command truth table
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped). See command truth table for details.

See JEDEC LRDIMM Specification.

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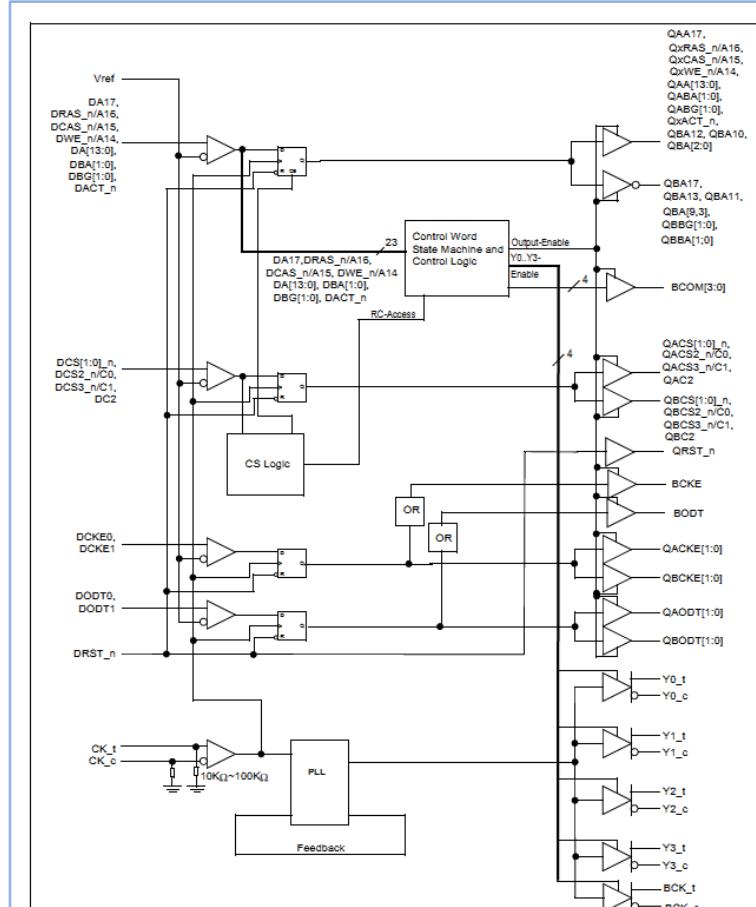
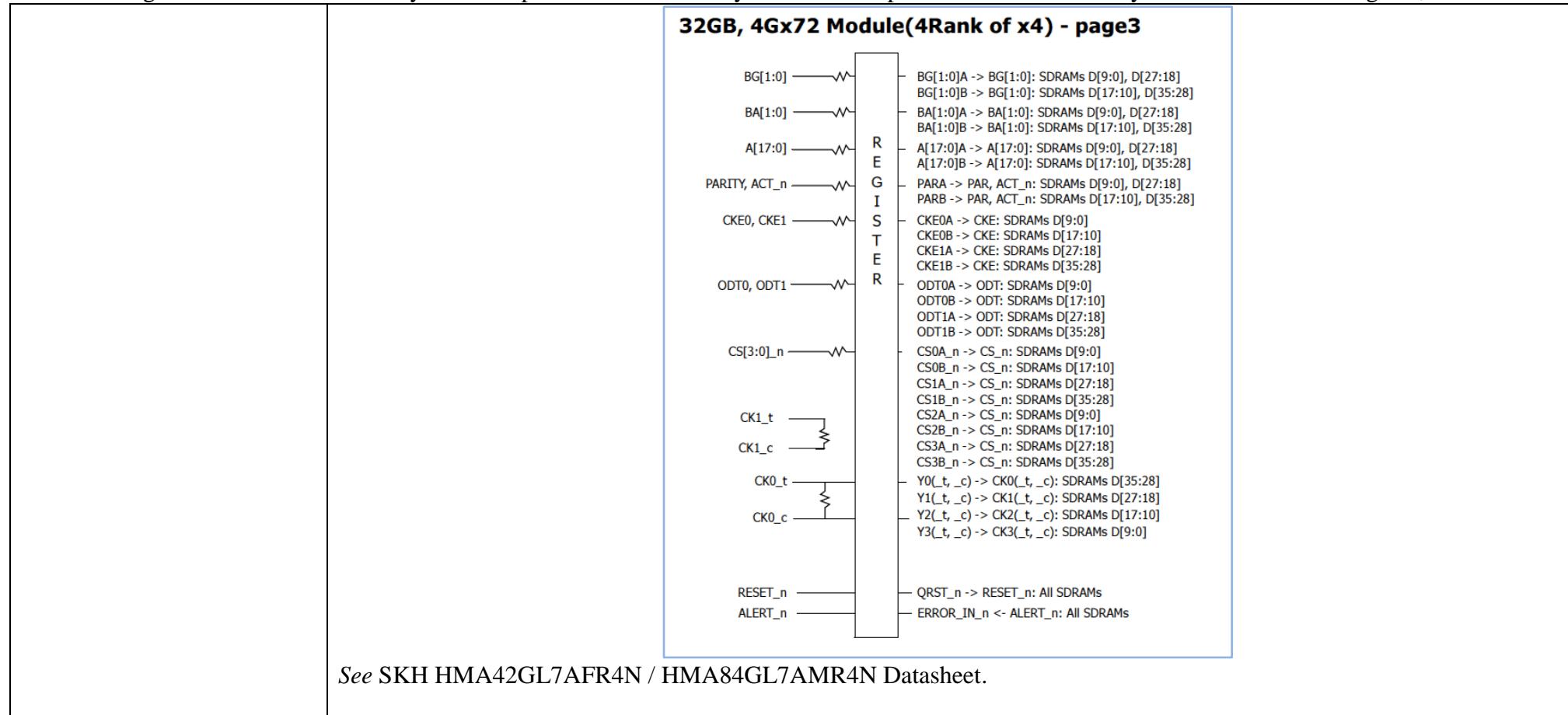


Figure 24 — Logic diagram (positive logic)

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

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2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n or DC0..DC1	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
Input Address and Command bus	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal.
	DA0..DA13, DAI7 DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
Clock inputs	CK_tCK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_tBCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

See JEDEC RCD01 Specification.

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/I, QAODT0/I, QBCKE0/I, QBODT0/I	CMOS ²	Register output CKE and ODT signals.
	QACS0_n, QACSI_n, QBCS0_n, QBCSI_n	CMOS ²	Register output Chip Select signals.
	QACS2_n, QACSI_n, QBCS2_n, QBCSI_n	CMOS ²	Register output Chip Select signals. These pins initiate DRAM address/command decodes.
	QAC0..QAC1, QBC0..QBC1	CMOS ²	Some of these have alternative functions: • QnCS2_n <=> QnC0 • QnCS3_n <=> QnC1
Output Address and Command bus	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QnA14 <=> QnWE_n • QnA15 <=> QnCAS_n • QnA16 <=> QnRAS_n
	QAACT_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers
Clock outputs	Y0_t, Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input

See JEDEC RCD01 Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

 4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 16 — Command Truth Table

Function	Abbreviation	CKE Prev- Cycle	CKE Current Cycle	CS_n	ACT_n	RAS_n IA1B	CAS_n IA1S	WE_n A14	BG0- BG1	BAD- BA1	C2-C0	A12/ BC_n	A17/ A11	A10/ AP	A0-A9	NOTE
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V			OP Code		12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	V	L	V
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	V	H	V
RFU	RFU	H	H	L	H	L	H	H			RFU					
Bank Activate	ACT	H	H	L	L		Row Address (RA)		BG	BA	V		Row Address (RA)			
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Pre- charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Pre- charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Pre- charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Pre- charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Pre- charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Pre- charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous to Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t_NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQLO-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DB/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert: It has multiple functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
NOTE: Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.		

See JEDEC DDR4 DRAM Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

	<p>2.2 Features and Functions</p> <p>The DDR4RCD01 has three basic modes of operation associated with the DA[1:0] bits in the DIMM Configuration Control Word (RCD0D):</p> <ul style="list-style-type: none">• In Direct DualCS mode (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. The inputs pins DC[2:0] are forwarded to two sets of output pins, QAC[2:0] and QBC[2:0]. This is the normal operating mode (“QuadCS disabled” and “Encoded CS disabled”).• In Direct QuadCS mode (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the “QuadCS enabled” mode.• In Encoded QuadCS mode (DA[1:0] = 11), two copies of four output chip selects, i.e., QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the “Encoded QuadCS” mode. <p>In the two modes above the DDR4 register does not need to decode input signals to generate any chip select outputs.</p>	
	<p><i>See JEDEC RCD01 Specification.</i> <i>See also JEDEC RCD02 Specification.</i></p>	

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.9 Output Inversion Enabling/Disabling

Output Inversion is enabled by default, after DRST_n is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs. The DDR4 register output signals are divided into two classes: signals that can be inverted (e.g., regular addresses) and signals that cannot be inverted (because they have a special function), see [Figure 18](#). Only the following 14 signals in the first class will be driven to the complement of the matching A-outputs: QBA3 to QBA9, QBA11, QBA13, QBA17, QBBA0 to QBBA1 and QBBG0 to QBBG1.

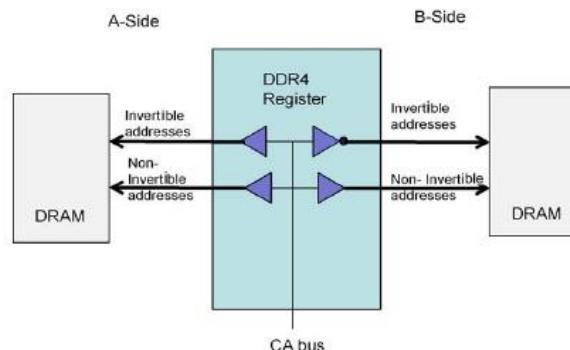


Figure 18 — Output Inversion Functional Diagram.

The Output Inversion feature is always enabled, even during DRAM MRS commands. In order to ensure that the DRAM receives the correct (i.e., uninverted) MRS bits, the host-to-register-to-DRAM MRS programming is split into a two-step process, see Figure 19. In the first step the A-side DRAMs are programmed using non-inverted addresses from the host. In the second step the B-side DRAMs are programmed using inverted addresses for the invertible address signals and non-inverted addresses for the non-invertible address signals from the host.

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.4 DDR4 SDRAM X4/8 Ballout using MO-207									
	1	2	3	4	5	6	7	8	9
A	VDD	VSSQ	TDQS_c ³		DM_n, DBI_n TDQS_t ² , (NC) ¹	VSSQ	VSS		A
B	VPP	VDDQ	DQS_c		DQ1	VDDQ	ZQ		B
C	VDDQ	DQ0	DQS_t		VDD	VSS	VDDQ		C
D	VSSQ	DQ4 (NC) ¹	DQ2		DQ3	DQ5 (NC) ¹	VSSQ		D
E	VSS	VDDQ	DQ6 (NC) ¹		DQ7 (NC) ¹	VDDQ	VSS		E
F	VDD	(C2) ⁵ ODT1 ⁶	ODT		CK_t	CK_c	VDD		F
G	VSS	(C0) ⁵ CKE1 ⁶	CKE		CS_n	(C1) ⁵ (CS1_n) ⁶	TEN (NC) ⁷		G
H	VDD	WE_n A14	ACT_n		CAS_n A15	RAS_n A16	VSS		H
J	VREFCA	BG0	A10 AP		A12 BC_n	BG1	VDD		J
K	VSS	BA0	A4		A3	BA1	VSS		K
L	RESET_n	A6	A0		A1	A5	ALERT_n		L
M	VDD	A8	A2		A9	A7	VPP		M
N	VSS	A11	PAR		A17 (NC) ⁴	A13	VDD		N

NOTE 1 These pins are not connected for the X4 configuration.

NOTE 2 TDQS_t is not valid for the x4 configuration.

NOTE 3 TDQS_c is not valid for the x4 configuration.

NOTE 4 A17 is only defined for the x4 configuration.

NOTE 5 These pins are for stacked component such as 3DS. For mono package, these pins are NC.

NOTE 6 ODT1 / CKE1 / CS1_n are used together only for DDP.

NOTE 7 TEN is optional for 8Gb and above. This pin is not connected if TEN is not supported.

Figure 1 — DDR4 Ball Assignments for the x4/8 component

See JEDEC DDR4 SDRAM Specification.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.11 Latency Equalization Support

3D Stacked SDRAMs have a higher CAS latency than monolithic devices. For greater platform flexibility it is highly desirable to mix DIMMs with both 3DS and mono SDRAMs on the same DDR4 channel. Since memory controllers typically can only handle devices with equal CAS latencies in the same channel, it is required that the DDR4 register has a mechanism to increase the CAS latency of mono SDRAMs to match the CAS latency of 3DS SDRAMs. However, this mechanism only equalizes the DRAM latencies, not the total DIMM latencies. Hence this DDR4 register mechanism does not by itself allow mixing DDR4 RDIMMs and DDR4 LRDIMMs in the same channel.

To equalize different SDRAM latencies, the DDR4 register supports a programmable latency adder of 0 nCK, 1nCK, 2nCK, 3nCK or 4nCK for all DRAM commands, see conceptual diagram in Figure 2.12. The power-up default is 1nCK latency adder.

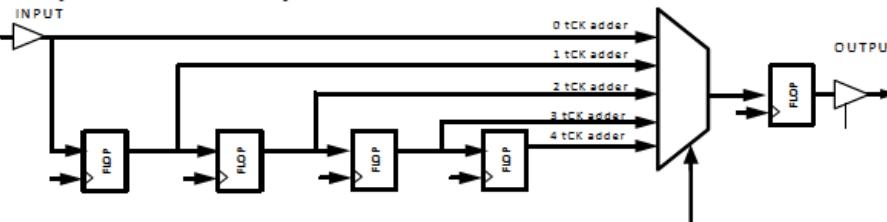


Figure 21 — Latency Equalizer Delays

See JEDEC RCD01 Specification.

See JEDEC RCD02 Specification.

2.5.2 Control Bus Timing

The output signals BCOM, BODT and BCKE are driven at the same time as the QxCA outputs, i.e., they are affected by the Command Latency Adder Control Word RC0F but a latency adder of 0 is not a valid configuration. For speeds above 2400MT/s, a minimum latency adder of 2 nCK is required in RC0F.

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

The data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller. For example, the IDT Data Buffers propagate data signals between the memory devices and the system memory controller during read and write commands.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

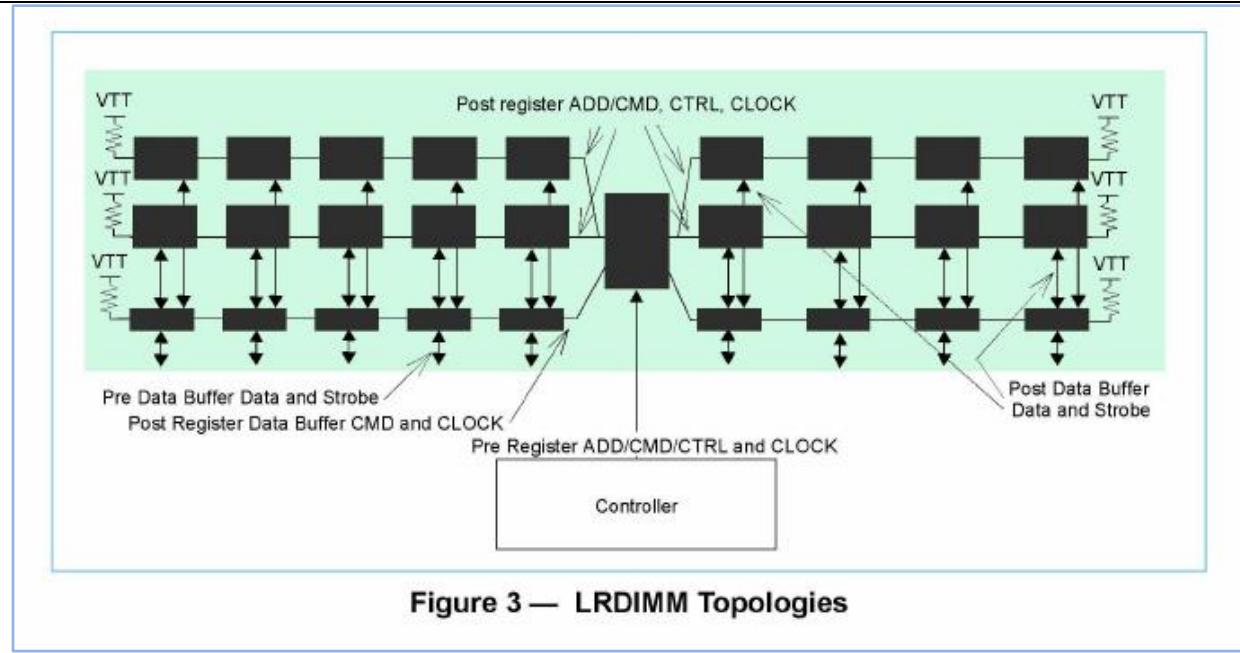


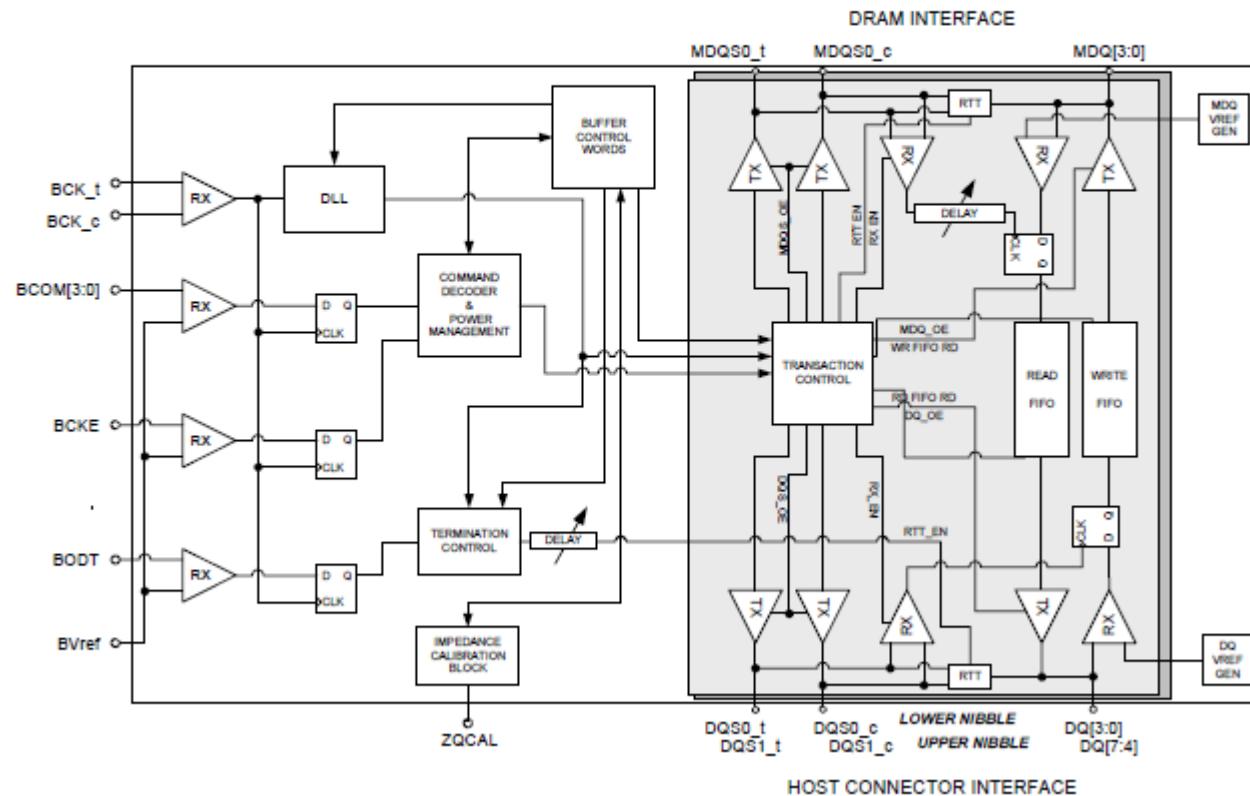
Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification.

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2.6 Logic Diagram

Figure 12 — Logic Diagram



See JEDEC DDR4 DB01 Standard Rev 1.0.

The one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals. For example, the first data signals are transmitted or received by the memory devices in response to read or write commands, respectively.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes..
	DCS1_n..DCS3_n or DC0..DC1	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
Input Address and Command bus	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal.
	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DA14..DA16	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
Clock inputs	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT1_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
Data buffer control and communication outputs	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

See JEDEC RCD01 Specification.

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Table 16 — Terminal functions

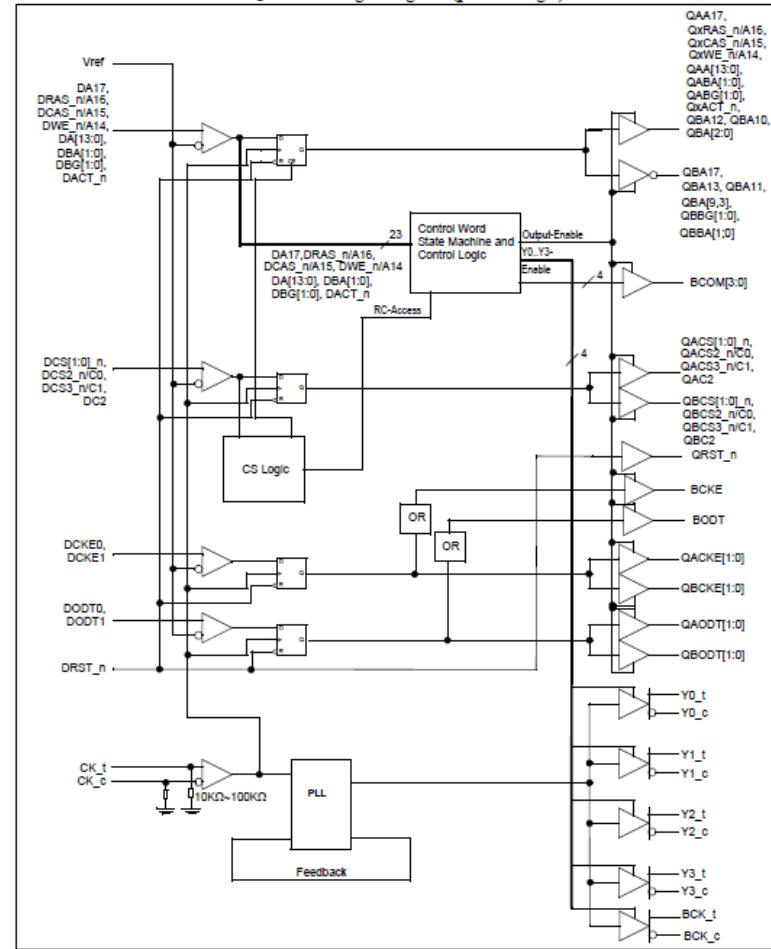
Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS ²	Register output CKE and ODT signals.
	QACSO_n, QACSI_n, QBCSO_n, QBCSI_n	CMOS ²	Register output Chip Select signals.
	QACS2_n, QACS3_n, QBCS2_n, QBCS3_n	CMOS ²	Register output Chip Select signals. These pins initiate DRAM address/command decodes.
	QAC0..QAC1, QBC0..QBC1		Some of these have alternative functions: • QnCS2_n <=> QnC0 • QnCS3_n <=> QnC1
	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAGO..QAG1, QBG0..QBG1	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n		In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QnA14 <=> QnWE_n • QnA15 <=> QnCAS_n • QnA16 <=> QnRAS_n
	QAACI_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input
	V _{DDSPD}	Power input	

See JEDEC RCD01 Specification.

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2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 16 — Command Truth Table

Function	Abbreviation	CKE	Prev- Row Cycle	Current Cycle	CS_n	ACT_n	RAS_n (A18)	CAS_n (A15)	WE_n	A14	BG0- BG1	BA0- BA1	C2-C0	A12/ BC_n	A17/ A15 A11	A10/ AP	AD-AS	NOTE
Mode Register Set	MRS	H	H	L	H	L	L	L	L	BG	BA	V			OP Code		12	
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	V	7,9	
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H						RFU				
Bank Activate	ACT	H	H	L	L		Row Address (RA)			BG	BA	V		Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	V	L	CA		
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA			
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA			
Write with Auto Pre- charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA			
Write with Auto Pre- charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA			
Write with Auto Pre- charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA			
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	V	L	CA		
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA			
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA			
Read with Auto Pre- charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA			
Read with Auto Pre- charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA			
Read with Auto Pre- charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA			
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	V	10	
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X		
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	6	
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	6	
ZQ calibration Long	ZQCL	H	H	L	H	H	L	V	V	V	V	V	V	V	H	V		
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	V	L	V		

See JEDEC DDR4 DRAM Specification.

Further, the RCD outputs signals via the BCOM bus to the DBs for Writes and Reads.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.1 Description

This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V VDD operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

All DQ inputs are pseudo-differential with an internal voltage reference. All DQ outputs are VDD terminated drivers optimized to drive single or dual terminated traces in DDR4 LRDIMM applications. The differential DQS strobes are used to sample the DQ inputs and are regenerated in the DDR4DB01 for driving out the DQ outputs on the opposite side of the device.

The clock inputs BCK_t and BCK_c are used to sample the control inputs BCOM[3:0], BCKE and BODT. The BCOM[3:0] inputs are used to write device internal control registers. The buffer control word (BCW) mechanism is described in more detail in Section 2.5.

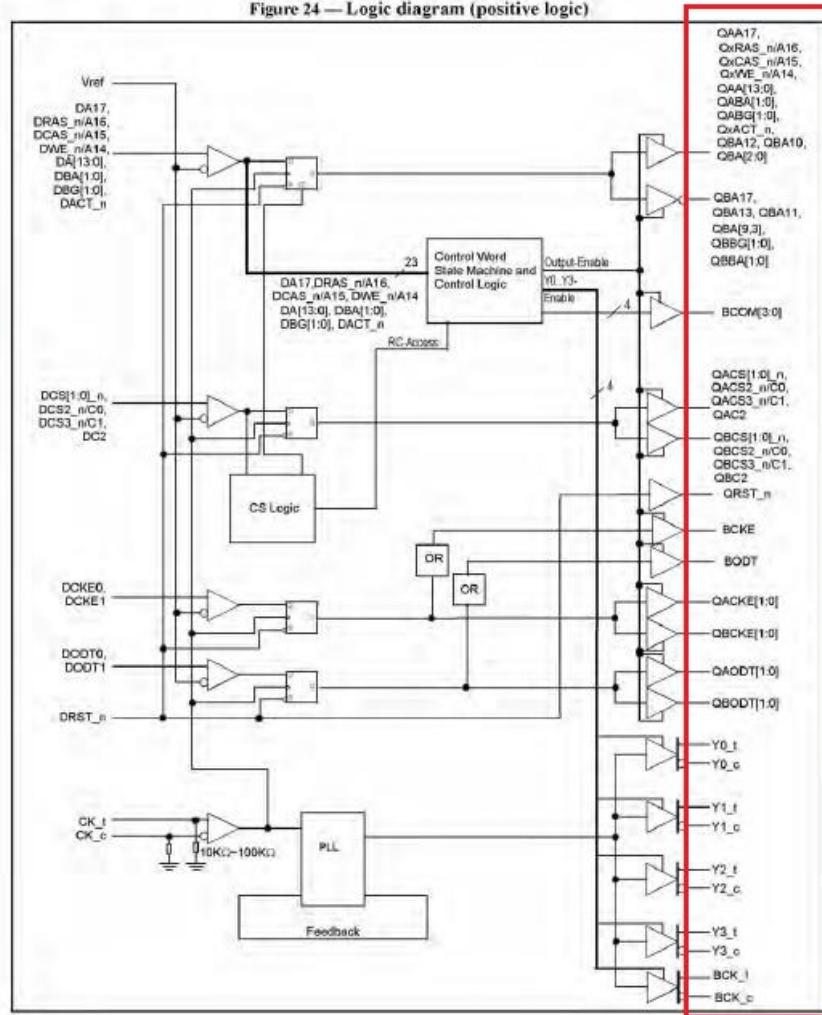
See DDR4DB01 Standard.

See also JEDEC DDR4 DB01 Standard Rev 1.0.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



See DDR4RCD01 Standard.

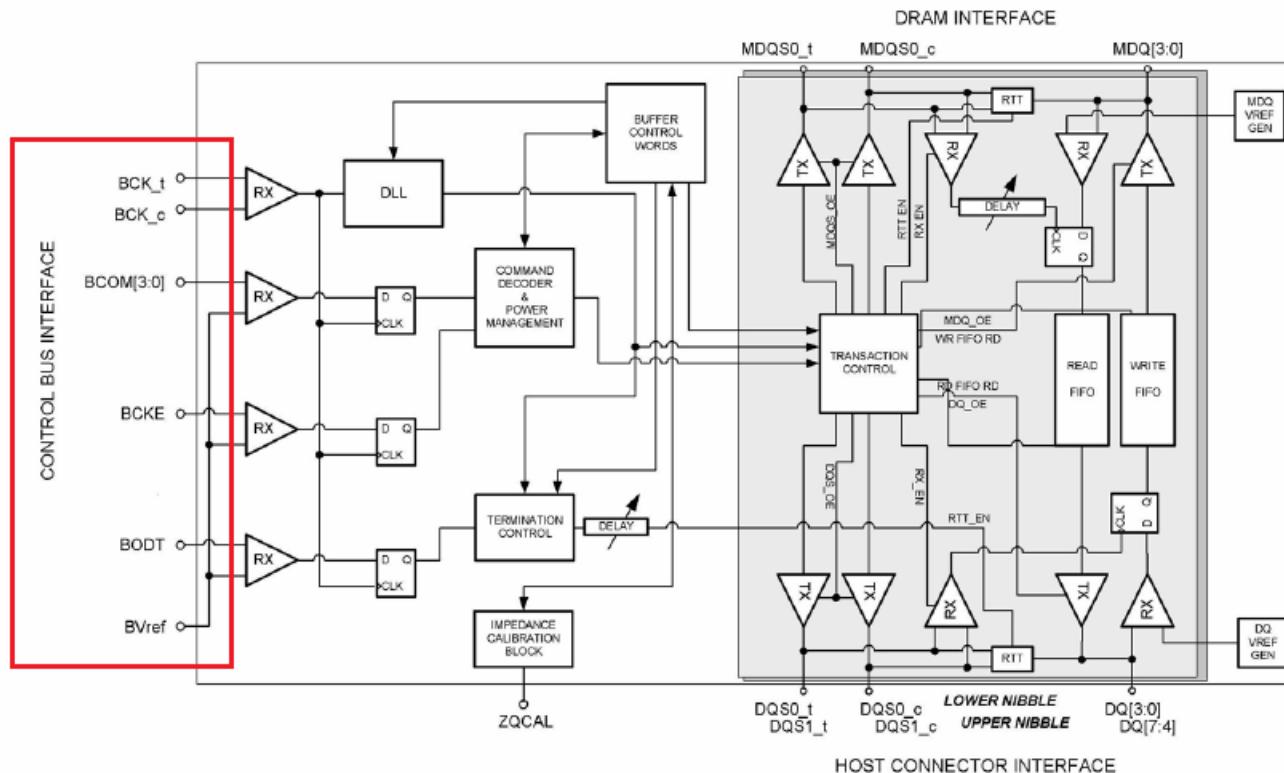
See JEDEC DDR4 RCD01 Standard Rev 1.0.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.17 Logic diagram

2.6 Logic Diagram

Figure 12 — Logic Diagram



See DDR4DB01 Standard.

See also JEDEC DDR4 DB01 Standard Rev 1.0.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

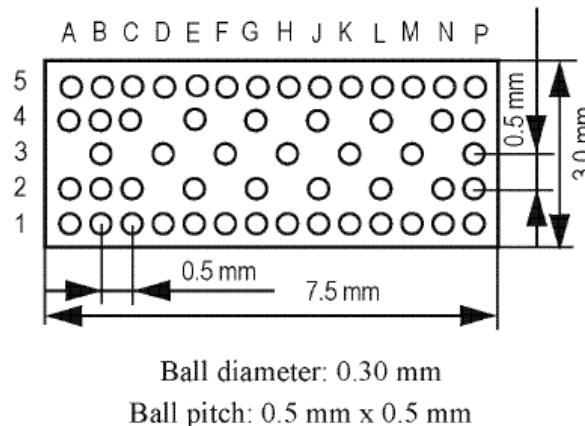


Figure 12 — 53 Ball Configuration 14 x5 (TOP VIEW)

Table 20 specifies the pinout for the DDR4DB02. The device has (mostly) symmetric pinout with host interface at the south side and DRAM interface at the north side.

Table 20 — Ball Assignment - 53-ball FBGA, 14 x 5 Grid, TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
5	BCOM3	BCOM2	MDQ3	MDQ2	MDQ7	MDQ6	MDQS0_t	MDQS0_c	MDQS1_c	MDQS1_t	MDQ1	MDQ0	MDQ5	MDQ4
4	BCOM0	BCOM1	V _{ss}		V _{ss}	ALERT_n								
3		V _{dd}		V _{dd}		V _{dd}		V _{dd}		V _{dd}		V _{dd}		BVrefCA
2	BCK_t	BCKE	V _{ss}		V _{ss}	ZQCAL								
1	BCK_c	BODT	DQ3	DQ2	DQ7	DQ6	DQS0_t	DQS0_c	DQS1_c	DQS1_t	DQ1	DQ0	DQ5	DQ4

See JEDEC BoD Ballot DDR4 DB02 Standard Rev 1.0.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.5 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DB). This interface is enabled on power-on and only disabled when the 'LRDIMM Disable' bit in the DIMM Configuration Control Word (RC0D) is set.

2.5.1 Control Bus Signals

Table 5 — List of Signals for Data Buffer control

Name	Description	Signal Count
BCOM[3:0]	Data buffer command signals	4
BCKE	Function of registered DCKE (dedicated non-encoded signal)	1
BODT	Function of registered DODT (dedicated non-encoded signal)	1
BCK_t, BCK_c	Clock outputs for the data buffers	2
BVrefCA	Reference voltage output for command and control signals connected to the data buffers	1
Total		9

See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.5.3 Control Bus Commands

2.5.3.1 Command List

Table 6 — Data Buffer Control Bus Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU ¹	Reserved for future use	1110
RFU ¹	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.5.4.1 Write Commands

Table 7 shows the sequence for write (WR4, WR8) commands. Each write command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. If CRC is enabled in the DRAM and in the DB (F4BC2x, DA7), the burst length will always be 10UI.

Table 7 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

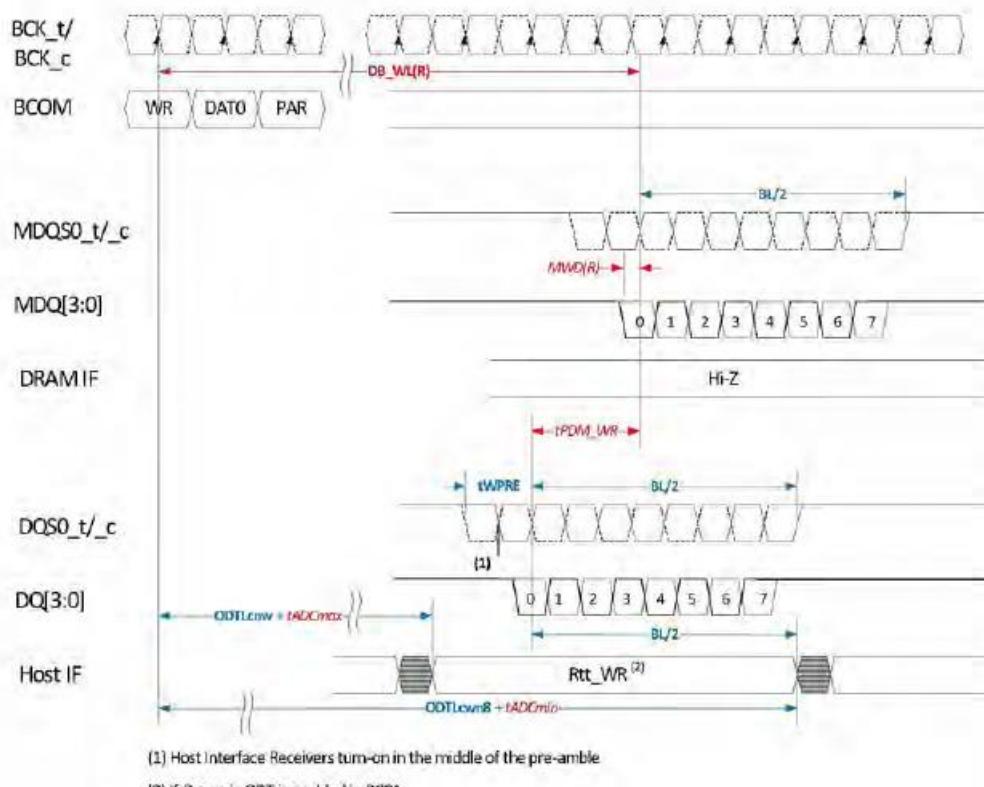


Figure 7 — WRITE Timing

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.5.5.2 Read Commands and MPR Override Reads

Table 8 shows the sequence for read (RD4, RD8) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MR0 snoop register is set for fixed burst length of 8 or 4 (A[1:0] = '00' or '10').

Table 8 — Multicycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001

Table 8 — Multicycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]. Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Figure 8 shows the timing sequence for a Read command.

"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

Figure 8 shows the timing sequence for a Read command.

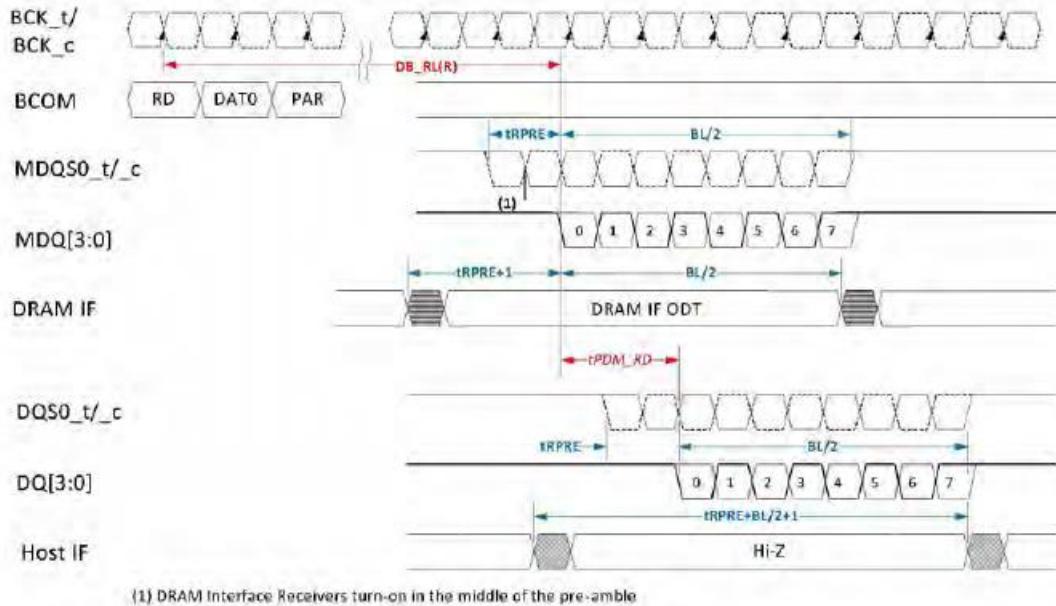


Figure 8—READ Timing

See JEDEC DDR4 RCD01 Standard Rev 1.0.

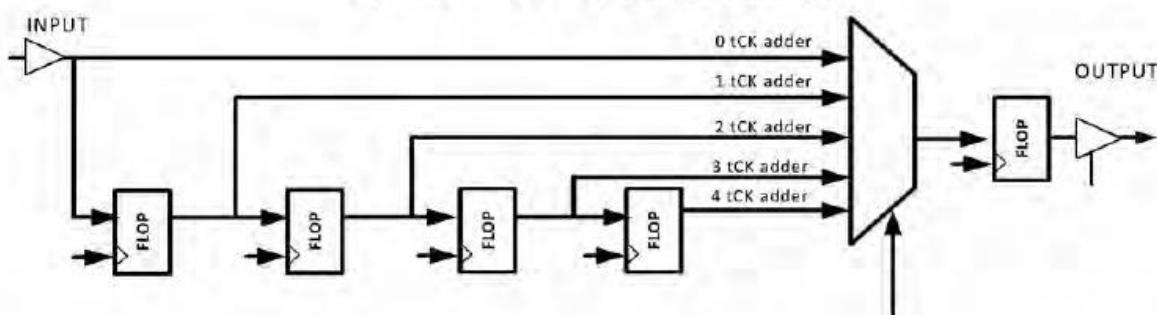
"wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and"

2.11 Latency Equalization Support

3D Stacked SDRAMs have a higher CAS latency than monolithic devices. For greater platform flexibility it is highly desirable to mix DIMMs with both 3DS and mono SDRAMs on the same DDR4 channel. Since memory controllers typically can only handle devices with equal CAS latencies in the same channel, it is required that the DDR4 register has a mechanism to increase the CAS latency of mono SDRAMs to match the CAS latency of 3DS SDRAMs. However, this mechanism only equalizes the DRAM latencies, not the total DIMM latencies. Hence this DDR4 register mechanism does not by itself allow mixing DDR4 RDIMMs and DDR4 LRDIMMs in the same channel.

To equalize different SDRAM latencies, the DDR4 register supports a programmable latency adder of 0 nCK, 1nCK, 2nCK, 3nCK or 4nCK for all DRAM commands - see conceptual diagram in Figure 2.12. The power-up default is 1nCK latency adder.

Figure 21 — Latency Equalizer Delays.



With a latency adder enabled, the DDR4 register will delay assertion of the QxCsN_n, QxCKEn, QxODTn, QxAn, QxBAn, QxBGn, QxACT_n, QxC2 and QxPAR outputs by the corresponding number of clock cycles.

See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module.	<p>The SK hynix Products are operable in a second mode wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module.</p> <p>The SK hynix Products are operable in a second mode wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices. For example, the SK hynix Products include a control module configured to output second memory address and control signals to the address and control ports of the memory devices while in DB-to-DRAM Write Delay ("MWD") Training Mode.</p>
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"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

2.1.8.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3 * 1/64 * tCK is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

See JEDEC DDR4 DB01 Standard Rev 1.0.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 16 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n/A15	CAS_n/A15	WE_n/A14	BG0-BG1	BA0-BA1	C2-C0	A12/BC_n	A17/A13/A11	A10/AP	AD-A9	NOTE
		Prev- cycle Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V			OP Code		12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	V
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H						RFU		
Bank Activate	ACT	H	H	L	L				Row Address (RA)	BG	BA	V		Row Address (RA)		
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Pre-charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Pre-charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	L	V	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NUT/DQSL_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/ A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP,A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge) A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW, burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .

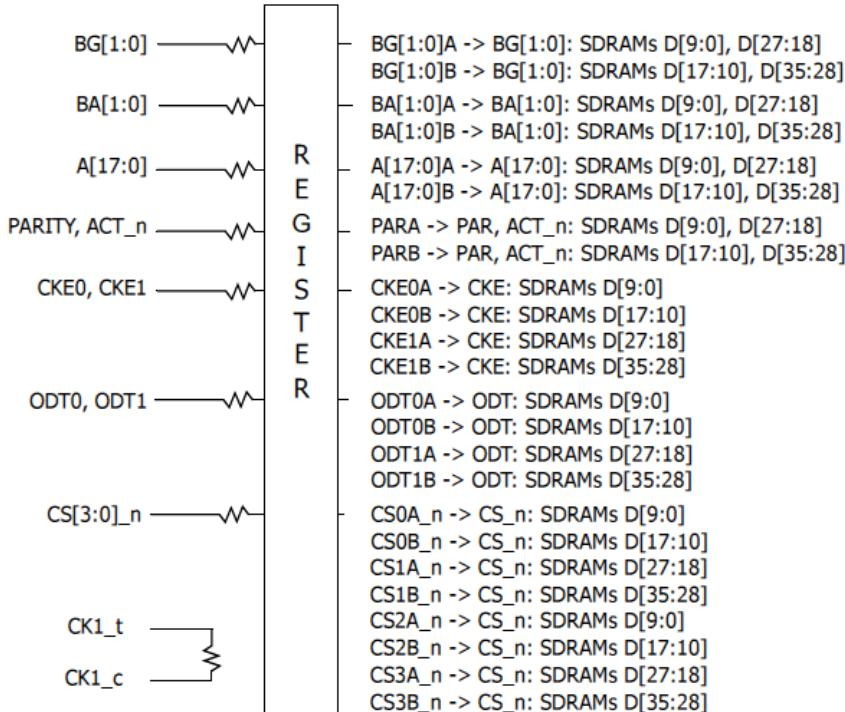
"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQ0-DQ7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DB/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert: It has multiple functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
NOTE: Input only pins (BG0-BG1,BA0-BA1,A0-A17,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT, and RESET_n) do not supply termination.		

See JEDEC DDR4 DRAM Specification.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

32GB, 4Gx72 Module(4Rank of x4) - page3



See HMA42GL7AFR4N/HMA84GL7AMR4N Datasheet.

CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
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See HMA42GL7AFR4N/HMA84GL7AMR4N Datasheet.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

		BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.	
		BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.	
		A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.	
<i>See HMA84GL7AMR4N Datasheet.</i>					

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n or DC0..DC1	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
Input Address and Command bus	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal.
	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n..DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
Clock inputs	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
	CK_tCK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_tBCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

See JEDEC RCD01 Specification.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

Table 16 — Terminal functions

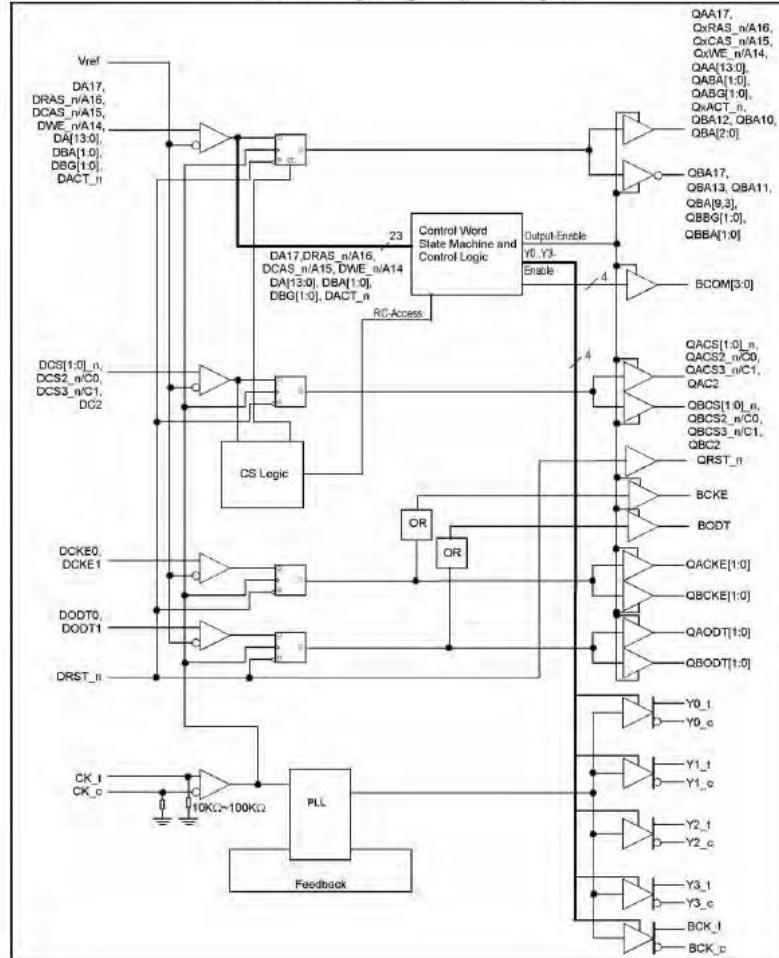
Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS ²	Register output CKE and ODT signals.
	QACS0_n, QACSI_n, QBCS0_n, QBCSI_n	CMOS ²	Register output Chip Select signals.
	QACS2_n, QACS3_n, QBCS2_n, QBCS3_n	CMOS ²	Register output Chip Select signals. These pins initiate DRAM address/command decodes. or QAC0..QAC1, QBC0..QBC1
	QAC1, QBC2	CMOS ²	Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1 Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QBA0..QBA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACI_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input

See JEDEC RCD01 Specification.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



See DDR4RCD01 Standard.

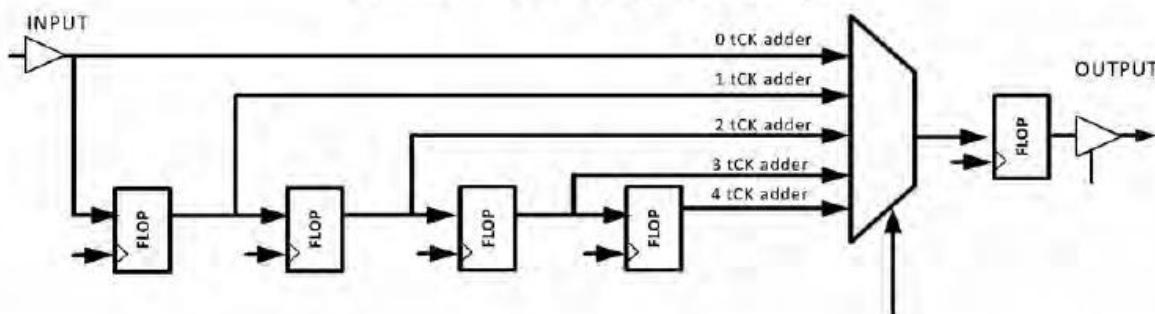
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2.11 Latency Equalization Support

3D Stacked SDRAMs have a higher CAS latency than monolithic devices. For greater platform flexibility it is highly desirable to mix DIMMs with both 3DS and mono SDRAMs on the same DDR4 channel. Since memory controllers typically can only handle devices with equal CAS latencies in the same channel, it is required that the DDR4 register has a mechanism to increase the CAS latency of mono SDRAMs to match the CAS latency of 3DS SDRAMs. However, this mechanism only equalizes the DRAM latencies, not the total DIMM latencies. Hence this DDR4 register mechanism does not by itself allow mixing DDR4 RDIMMs and DDR4 LRDIMMs in the same channel.

To equalize different SDRAM latencies, the DDR4 register supports a programmable latency adder of 0 nCK, 1nCK, 2nCK, 3nCK or 4nCK for all DRAM commands - see conceptual diagram in Figure 2.12. The power-up default is 1nCK latency adder.

Figure 21 — Latency Equalizer Delays.



With a latency adder enabled, the DDR4 register will delay assertion of the QxC_n, QxCKEn, QxODTn, QxAn, QxBAn, QxBGn, QxACT_n, QxC2 and QxPAR outputs by the corresponding number of clock cycles.

See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

The data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller. For example, in the second mode, the host-to-DB path is not used to perform read and write operations between the data buffers and the memory devices.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

2.1.8.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3 * 1/64 * tCK is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

See JEDEC DDR4 DB01 Standard Rev 1.0.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

The SK hynix Products transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module. For example, the IDT data buffers transmit data signals to and from the data ports of the memory devices during DB-to-DRAM Write Delay mode according to BCW write and read commands (sent from the RCD), respectively.

2.5.3 Control Bus Commands

2.5.3.1 Command List

Table 6 — Data Buffer Control Bus Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU ¹	Reserved for future use	1110
RFU ¹	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

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2.5.5.4 BCW Write Command

Table 10 shows the sequence for buffer control word write commands.

Table 10 — Multicycle Sequence for BCW Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Write	Buffer control word write access command BCOM[3:0] = 1100
2	DAT0	First data transfer for BCW Write command BCOM[3:0] = {0, DA2, DA1, DA0}
3	DAT1	Second data transfer for BCW Write command BCOM[3:0] = {0, DA5, DA4, DA3}
4	DAT2	Third data transfer for BCW Write command BCOM[3:0] = {0, DA8, DA7, DA6}
5	DAT3	Fourth data transfer for BCW Write command BCOM[3:0] = {0, DA11, DA10, DA9}
6	DAT4	Fifth data transfer for BCW Write command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW writes BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW writes BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW writes BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW writes BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW writes BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW writes BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW writes BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW writes
7	PAR[3:0]	Even parity bits for BCW Write command and data PAR[x]: parity bit for 6 previous BCOM[x] transfers
8	Next Cmd	Next Command

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

The sequence for a BCW Write command is shown in Figure 10 below. The timing diagrams show how the BCW Write command is followed by five data transfer cycles and a parity data transfer cycle. Since the command sequence uses seven cycles it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the BCW Write command to the following valid command (also shown in the diagrams).

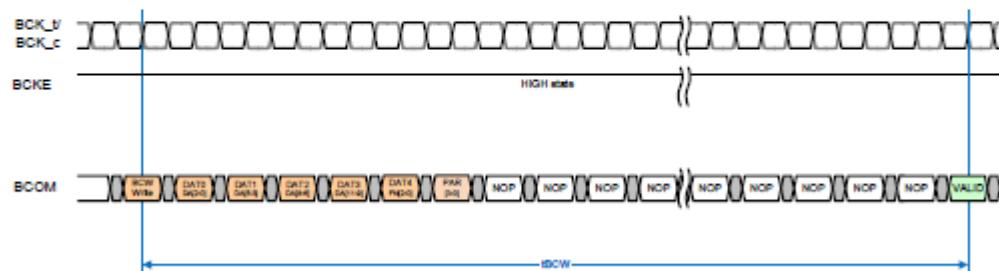


Figure 10 — Buffer Control Word Write command sequence

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

2.5.5.5 BCW Read Commands

The DDR4RCD01 generates a BCW Read command on the buffer control bus when it receives a CW Read command in RC06 with A12 = 1.

Table 11 shows the sequence for BCW Read commands.

Table 11 — Multicycle Sequence for BCW Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Read	Buffer control word read access command BCOM[3:0] = 1101
2	DAT0	First data transfer for BCW Read command BCOM[3:0] = {0, DA5, DA4, 0}
3	DAT1	Second data transfer for BCW Read command BCOM[3:0] = {0, DA8, DA7, DA6}
4	DAT2	Third data transfer for BCW Read command BCOM[3:0] = {0, DA11, DA10, DA9}
5	DAT3	Fourth data transfer for BCW Read command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW reads BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW reads BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW reads BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW reads BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW reads BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW reads BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW reads BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW reads
6	PAR[3:0]	Even parity bits for BCW Read command and data PAR[x]: parity bit for 5 previous BCOM[x] transfers
7	Next Cmd	Next Command

The sequence for BCW Read command is shown in Figure 11 below. The timing diagrams show how the BCW Read command is followed by four data transfer cycles and a parity data transfer cycle. This BCW Read command moves the selected BCW bits to MPR0 and configures the DB for MPR override read mode for the next Read command. The DB treats the first Read command after a BCW Read command as an MPR0 override read (regardless of the BCOM[1:0] bits during the DAT0 cycle of the corresponding BCOM Read command). The read data is driven out after DB_RL(R0) on the host interface DQ pins after the Read command. Just like in regular MPR override read mode, DDR4RCD01 will forward Read command to DRAM but DDR4DB01 will ignore read data from DRAM.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

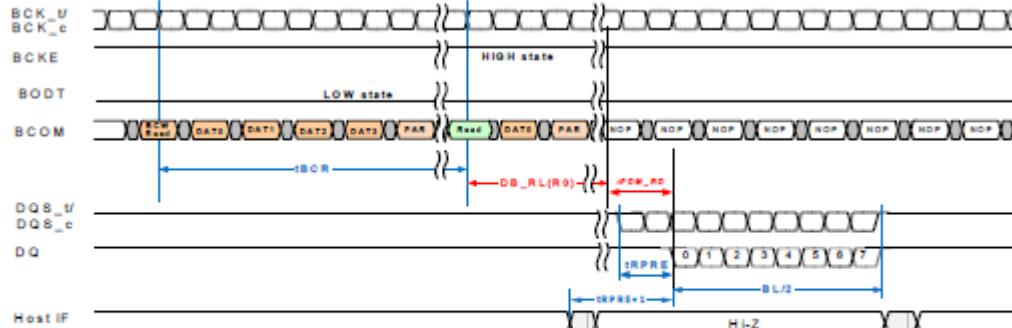


Figure 11 — BCW Read command sequence

See JEDEC DDR4 RCD01Standard Rev 1.0.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

2.1.8.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3 * 1/64 * tCK is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

See JEDEC DDR4 DB01 Standard Rev 1.0.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

	At least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module. For example, the IDT RCD sends address and control signals (as part of read and write commands) to the memory devices so that they can receive one or more data signals from the IDT Data Buffers.
--	---

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

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For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3 * 1/64 * tCK is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

See JEDEC DDR4 DB01 Standard Rev 1.0.

"wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module."

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

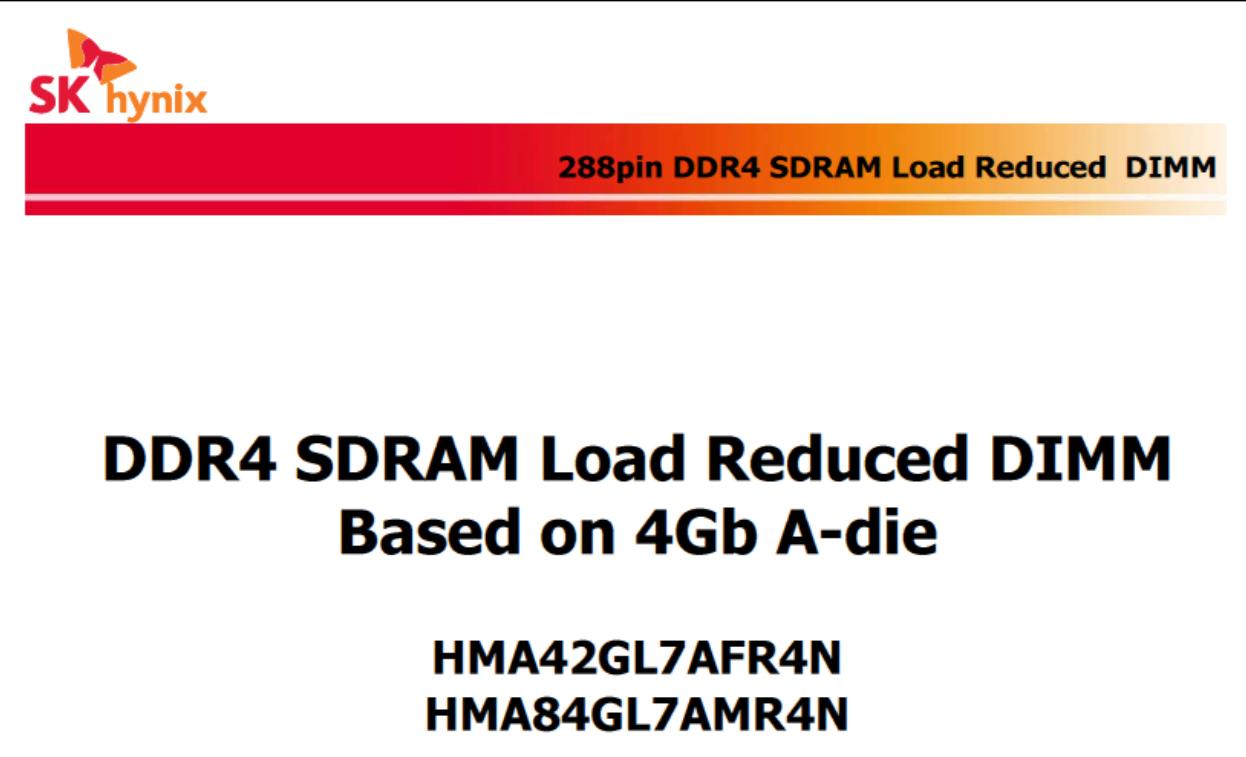
[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 16 — Command Truth Table

Function	Abbreviation	CKE										C2-C0	A1(2)/BC_n	A17/A15/A11	A19/AP	AD-AS	NOTE
		Prev. cycle	Current Cycle	CS_n	ACT_n	RAS_n/A18	CAS_n/A15	WE_n/A14	BG0-BG1	BAD-BAT							
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12	
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	V	V
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	7,8,9,10
Single Bank Precharge	PRE	H	H		L	H	L	H	BG	BA	V	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU								
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)					
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA		
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA		
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA		
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA		
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA		
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA		
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA		
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA		
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA		
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA		
Read with Auto Pre-charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA		
Read with Auto Pre-charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA		
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	5
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V		
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V		

See JEDEC DDR4 DRAM Specification.

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"

19. A memory module operable in a computer system with a system memory controller, the memory module comprising:	<p>The SK hynix Products are memory modules operable in a computer system with a system memory controller. For example, the SK hynix Products are DDR4 load reduced dual in-line memory modules ("LRDIMM").</p>  <p>(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).</p>  <p>See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet, at 1.</p>
--	---

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"



Description

SK hynix Load Reduced DDR4 SDRAM DIMMs are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Load Reduced DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

Features

- 288 pin Load Reduced DDR4 DRAM Dual In-Line Memory Modules
- Buffer performance by LRDIMM presenting less load to system

See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 3 (annotation added).

JEDEC Standard No. 21C
Page 4.20.27-1

4.20.27 - 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/
PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification

DDR4 SDRAM Load Reduced DIMM Design Specification

Revision 1.00

August 2015

See JEDEC LRDIMM Specification.

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"

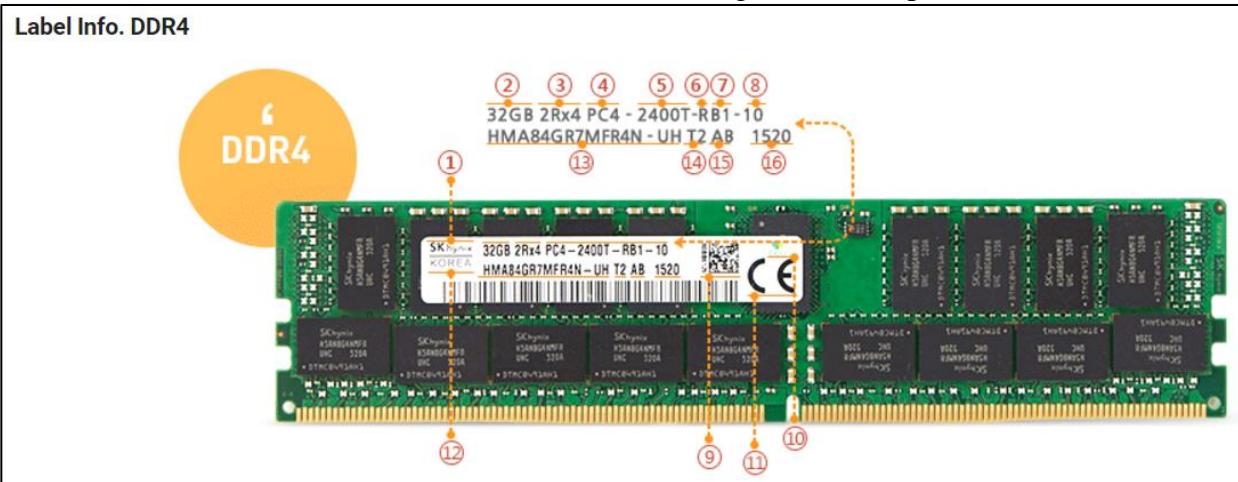
JEDEC Standard No. 21C
Page 4.20.27-5

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.

See JEDEC LRDIMM Specification (annotation added).

The SK hynix HMA84GL7AMR4N-UHTE is manufactured according to JEDEC specifications:



See SKH DDR4 Module Label Info at 3.

(6)	Module Type	U : 288pin Unbuffered DIMM R : 288pin Registered DIMM S : 260 pin Unbuffered SO-DIMM L : 288pin LRDIMM N : 288pin NVDIMM
(7)	Gerber Revision	JEDEC Reference design file used for this design
(8)	SPD Revision	JEDEC SPD Revision Encoding and Additions level

See SKH DDR4 Module Label Info at 3.

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).

DDR4 Load Reduced DIMM Design File

Raw Card	Applicable Design File	Applicable BOM
D0	PC4-LRDIMM_V050_RC_D0_20130828.brd	PC4-LRDIMM_V050_RC_D0_20130828_BOM.xlsx
D1	PC4-LRDIMM_V070_RC_D1_20141106.brd	PC4-LRDIMM_V070_RC_D1_20141106_BOM.xlsx
D2	PC4-LRDIMM_RC_D2_R050_V200_20160229.brd	PC4-LRDIMM_RC_D2_R050_V200_20160229_BOM.xlsx

See JEDEC Annex D - Raw Card D at 1.

The SK hynix Products are intended for use as main memory in computer systems such as servers and workstations.

JEDEC Standard No. 21C
Page 4.20.27-5

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.

See JEDEC LRDIMM Specification (annotation added).

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"

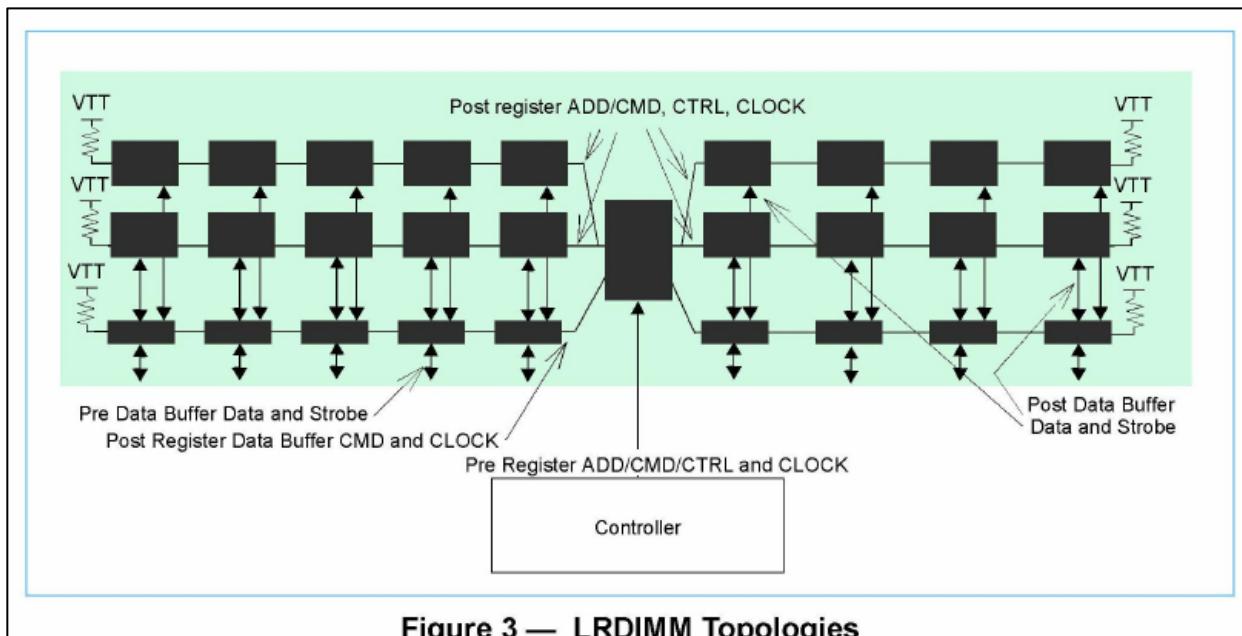


Description

SK hynix Load Reduced DDR4 SDRAM DIMMs are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Load Reduced DIMMs are intended for use as main memory when installed in systems such as servers and workstations.

See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 3 (annotations added).

The SK hynix Products are operable in a computer system with a system memory controller. For example, the SK hynix Products include a printed circuit board (PCB) for communicating signals between (e.g., to/from) the memory module and the memory controller of a computer system.



JEDEC LRDIMM Specification.

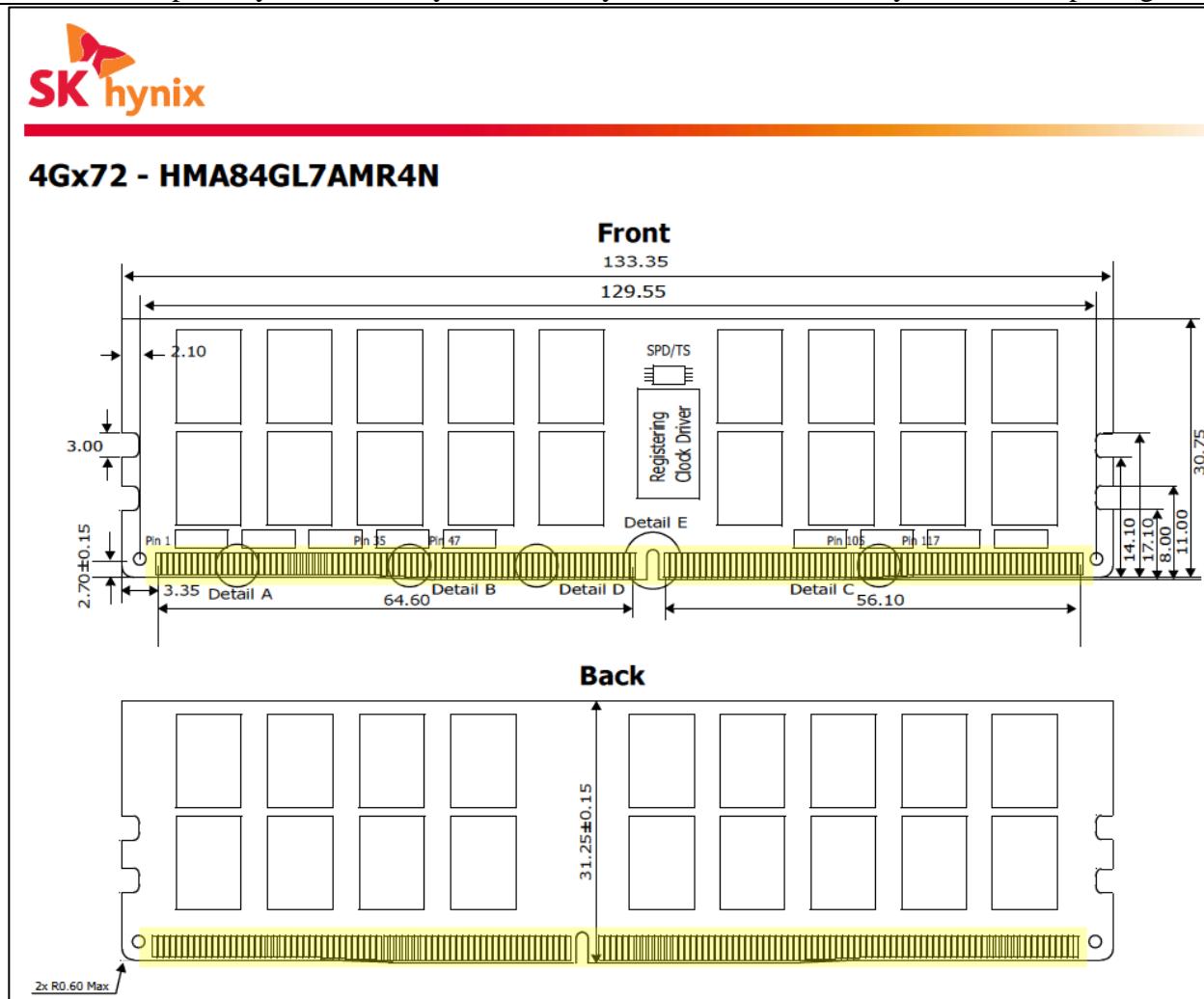
For example, the SK hynix Products contain contacts for connecting to a memory controller of a computer system.

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE)

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"



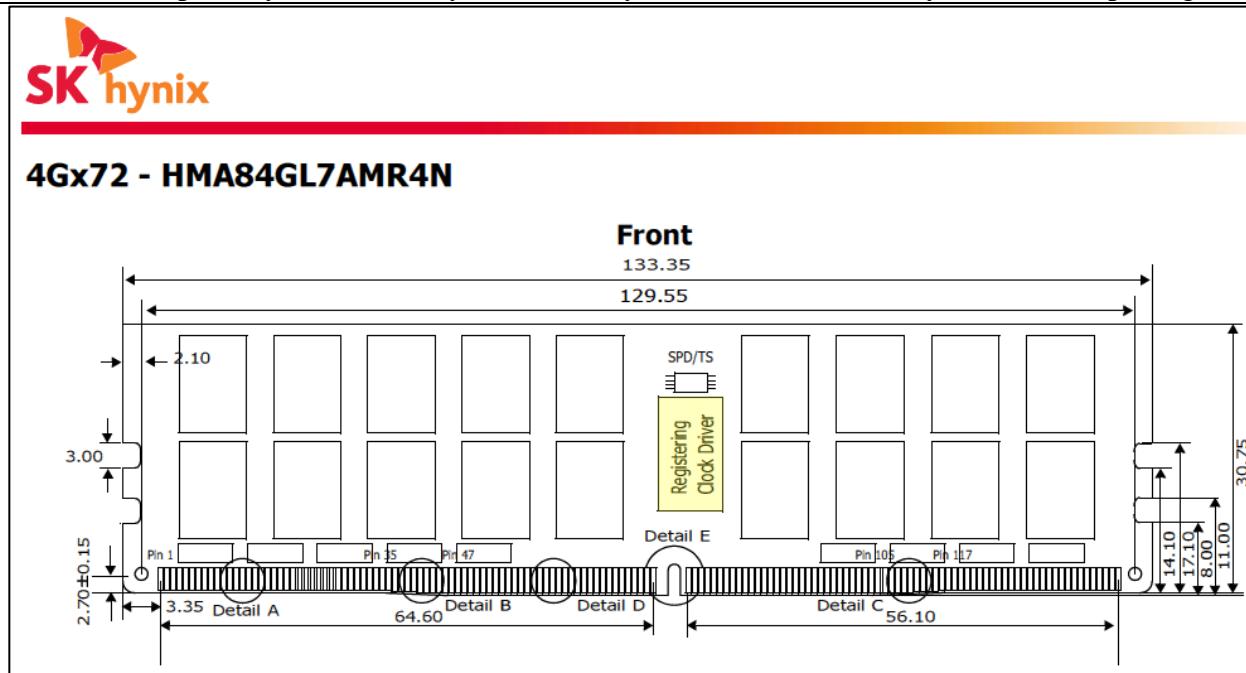
SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 65 (annotations added).

Further, the SK hynix include a JEDEC-compliant register clock driver ("RCD") that is operable with a memory controller of a computer system.

Some modules have lower current requirements. Any specific module must meet the SDRAM, **DDR4RCD01**, and **DDR4DB01** voltage requirements for its worst case supply currents.

See, e.g., JEDEC LRDIMM Specification (annotation added).

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"



SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 65 (annotations added).

Specifically, the SK hynix Products contain a IDT 4RCD0124KC0 RCD.



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).

The IDT 4RCD0124KC0 RCD is JEDEC Compliant.

Features

- JEDEC Compliant RCD

See 4RCD0124K DDR4 Register Clock Driver Webpage at 1.

BENEFITS

- All devices are JEDEC® compliant and meet stringent requirements for reliability and application compliance

IDT Leader in Server Memory Chipsets at 1.

The SK hynix Products further comply with the JEDEC SDRAM Standard, JESD79-4.

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"

**JEDEC
STANDARD**

DDR4 SDRAM

JESD79-4A

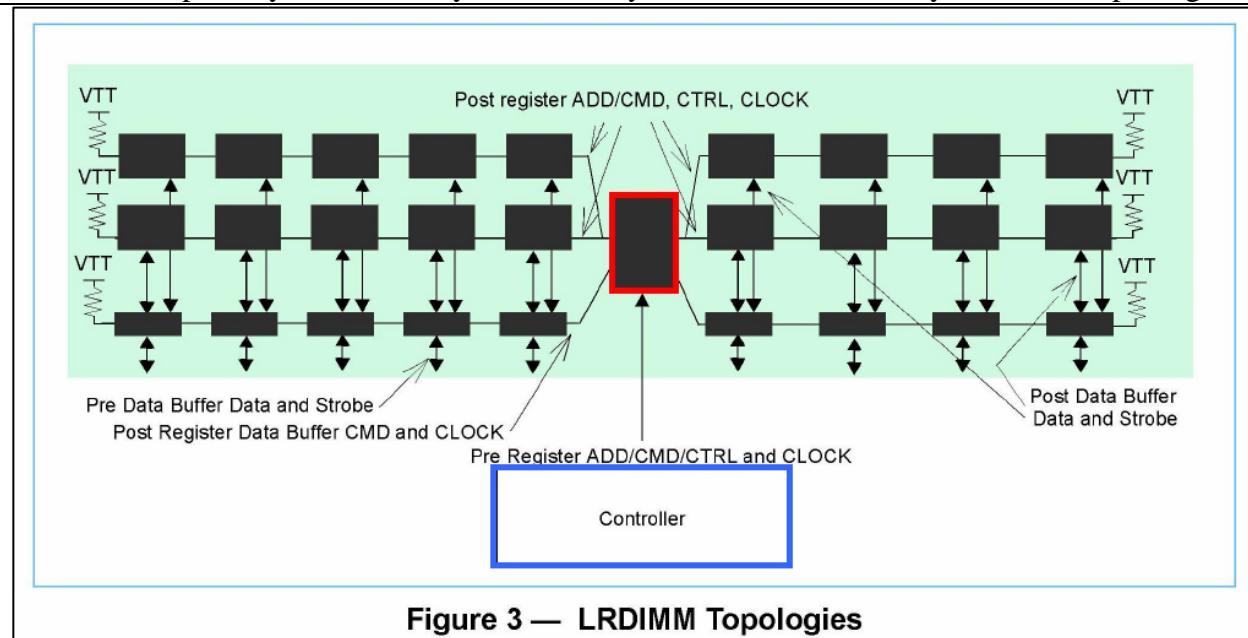
(Revision of JESD79-4, September 2012)

JEDEC DDR4 SDRAM Specification (annotations added).

See also SKH DDR4 Device Operation at 1.

The RCD is operatively coupled to the memory controller of the host system.

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"



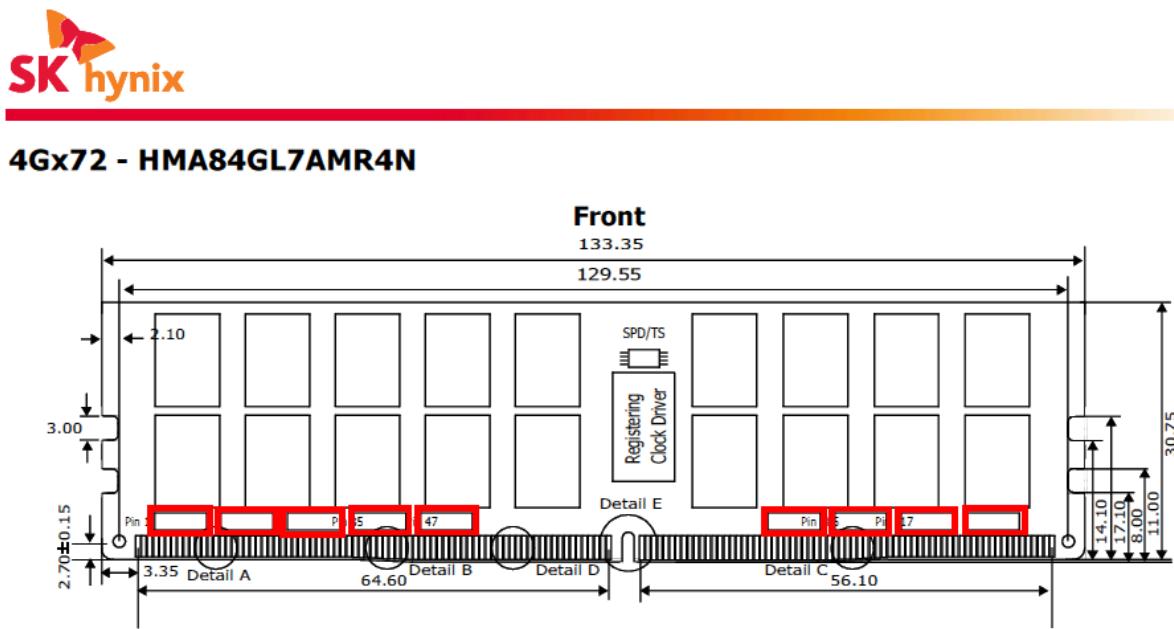
JEDEC LRDIMM Specification (annotations added).

Further, the SK Hynix Products include a plurality of IDT 4DB0226KA3AVG8 Data Buffers. The below picture of the SK Hynix HMA84GL7AMR4N-TFTE AB DIMM is representative of the SK Hynix LRDIMM Products and the data buffers they include.



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-TFTE AB).

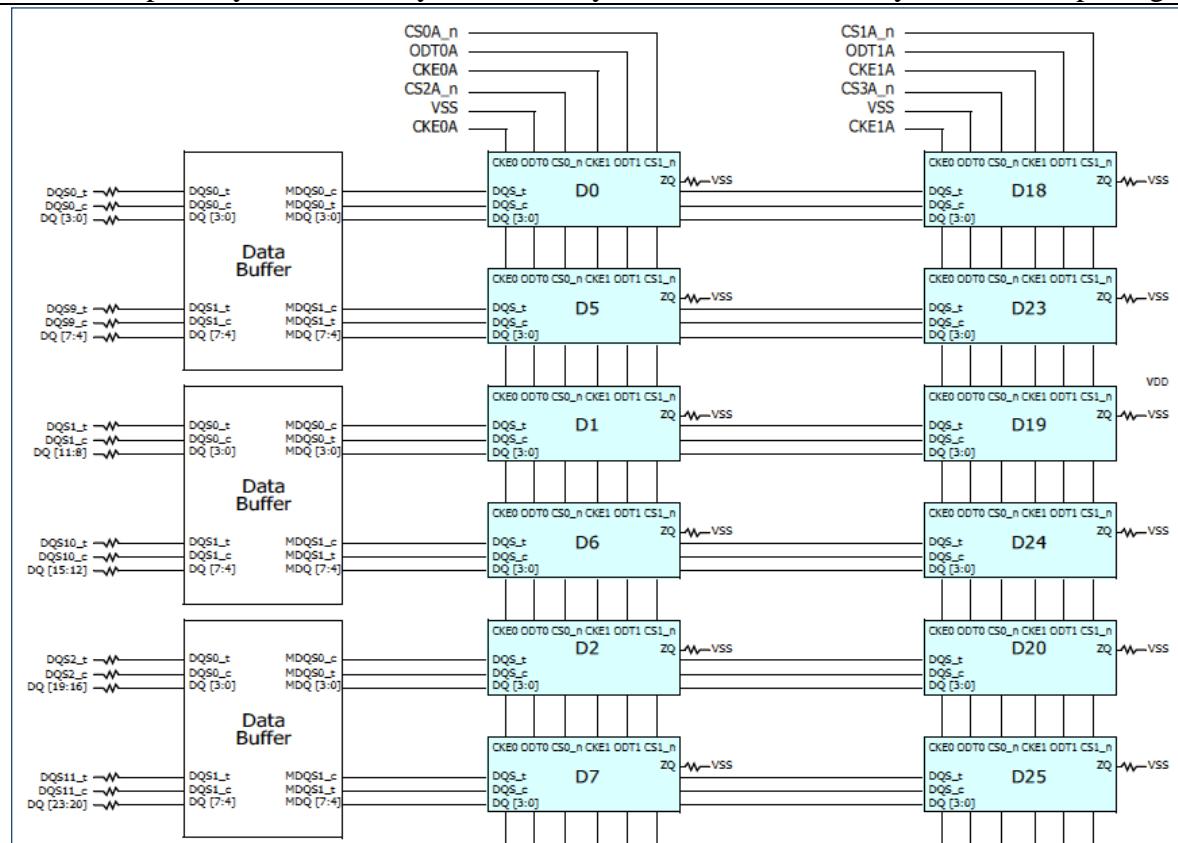
"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"



See HMA84GL7AMR4N Datasheet.

The data buffers are coupled between the data ports of the memory devices and the system memory bus.

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"



See HMA84GL7AMR4N Datasheet

2.1 Description

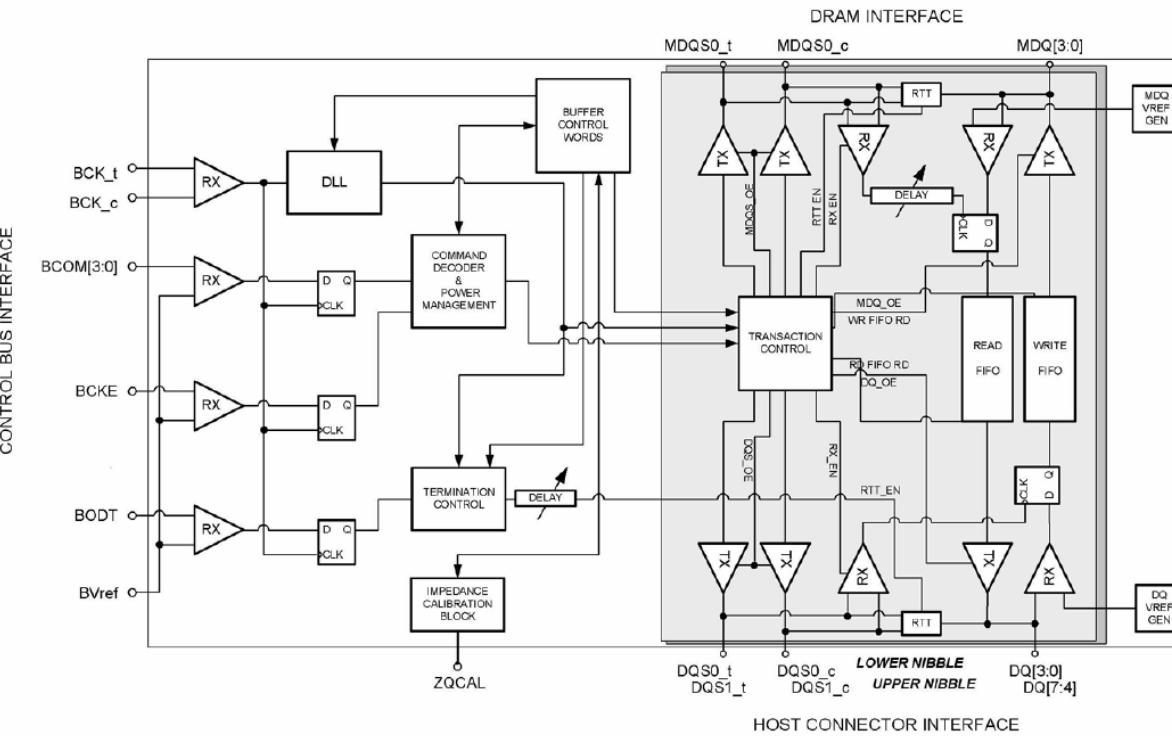
This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V VDD operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

See DDR4DB01 Standard

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"

2.6 Logic Diagram

Figure 12 — Logic Diagram



See DDR4DB01 Standard

"19. A memory module operable in a computer system with a system memory controller, the memory module comprising:"

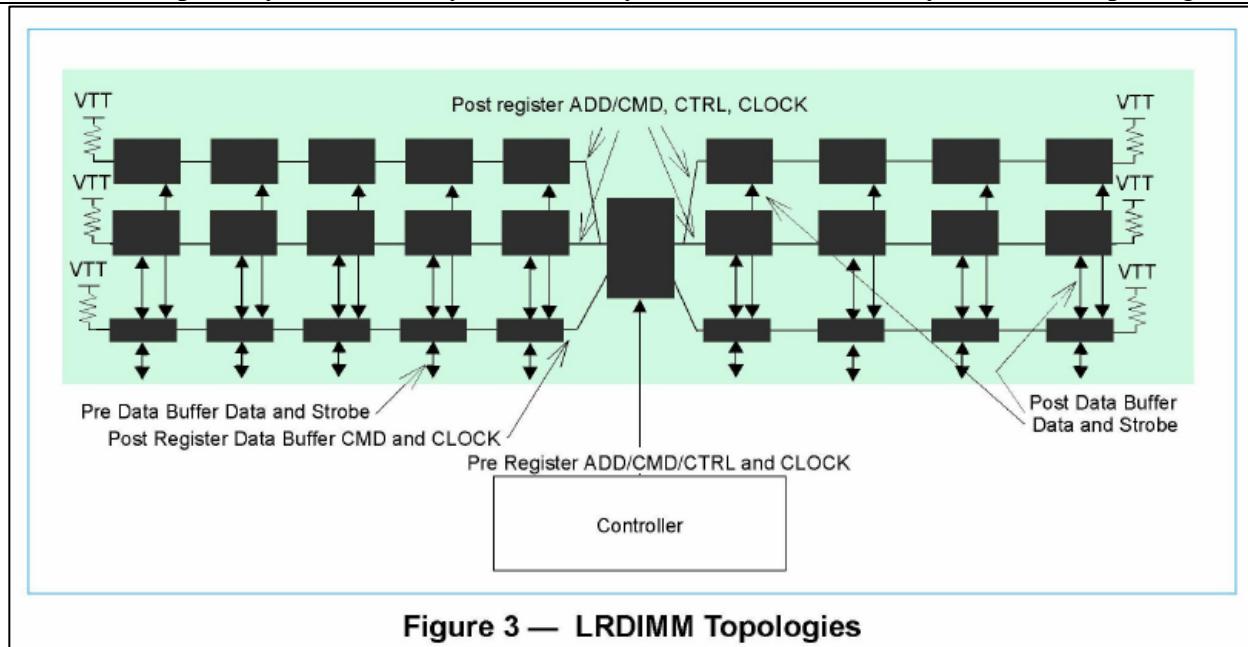


Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification.

"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"

<p>a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;</p>	<p>The SK hynix Products comprise a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller.</p> <p>The SK hynix Products include a printed circuit board (PCB) configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller.</p> <p>For example, the PCB of the SK hynix Products is configured to fit into a corresponding slot of the host system.</p> <div style="border: 1px solid black; padding: 10px;">  <h3>Description</h3> <p>SK hynix Load Reduced DDR4 SDRAM DIMMs are low power, high-speed operation memory modules that use DDR4 SDRAM devices. These Load Reduced DIMMs are intended for use as main memory when installed in systems such as servers and workstations.</p> </div> <p><i>See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 3 (annotation added).</i></p> <div style="border: 1px solid black; padding: 10px;"> <p style="text-align: right;">JEDEC Standard No. 21C Page 4.20.27-5</p> <h3>1 Product Description</h3> <p>This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.</p> </div> <p><i>See JEDEC LRDIMM Specification (annotation added).</i></p> <p>For example, as illustrated in the figures below, the SK hynix Products include a printed circuit board (PCB) having edge connections for communicating signals between (e.g., to/from) the memory module and the memory controller of the host system, e.g., electrical communication between the memory module and the memory controller.</p>
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"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"

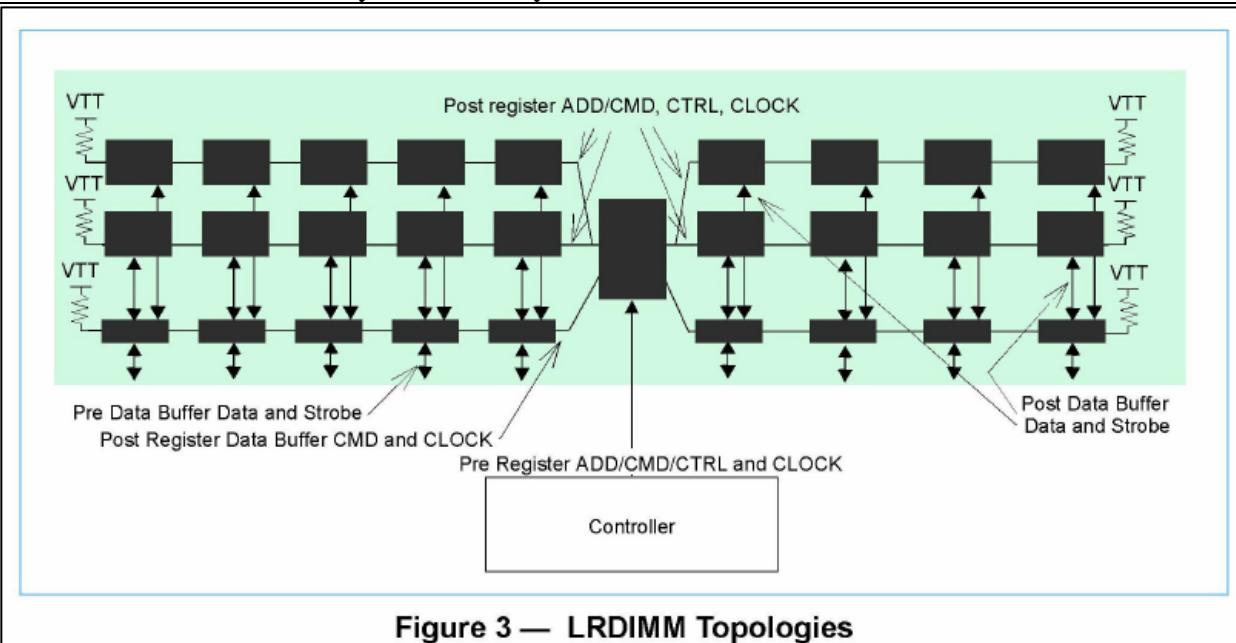


Figure 3 — LRDIMM Topologies

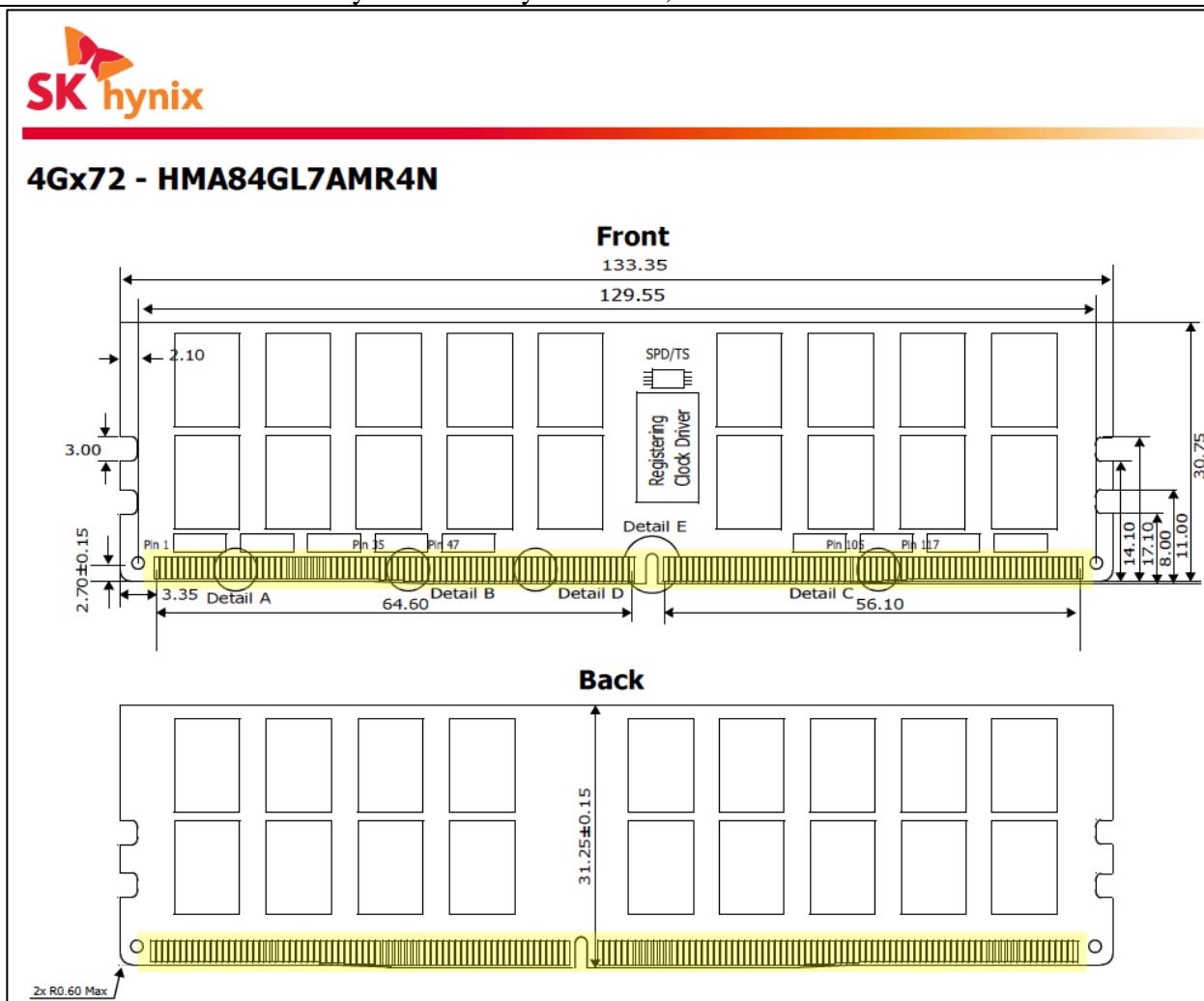
JEDEC LRDIMM Specification.

For example, the SK hynix Products contain contacts (e.g., edge connections) for connecting to a memory controller of a computer system.



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE)

"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"



See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 65 (annotations added).

The connector is further configured to provide an electrical connection for data signals between the memory module and the system memory controller. For example, the DQ and DQS signals are used to communicate data signals between the memory module and the memory controller of the computer system.

"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"

JEDEC Standard No. 21C
Page 4.20.27-17

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into seven groups. Figure 3 summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. The signal groups are:

1. DQ and DQS signals connector to Data Buffer (DB)
2. DQ and DQS signals DB to SDRAM

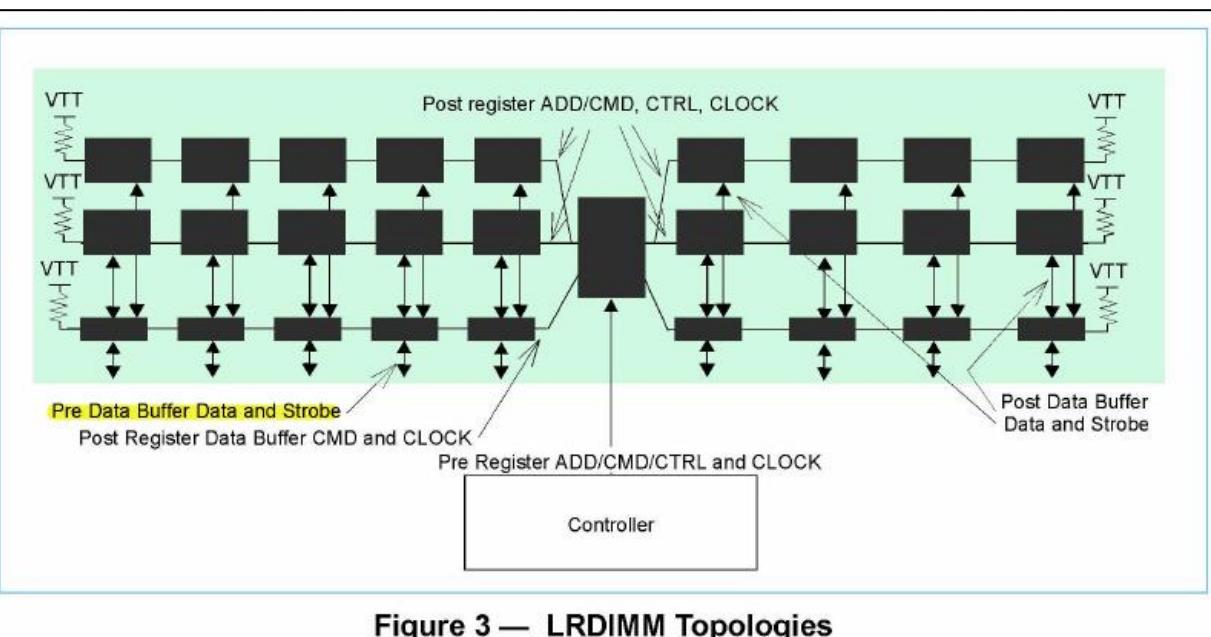


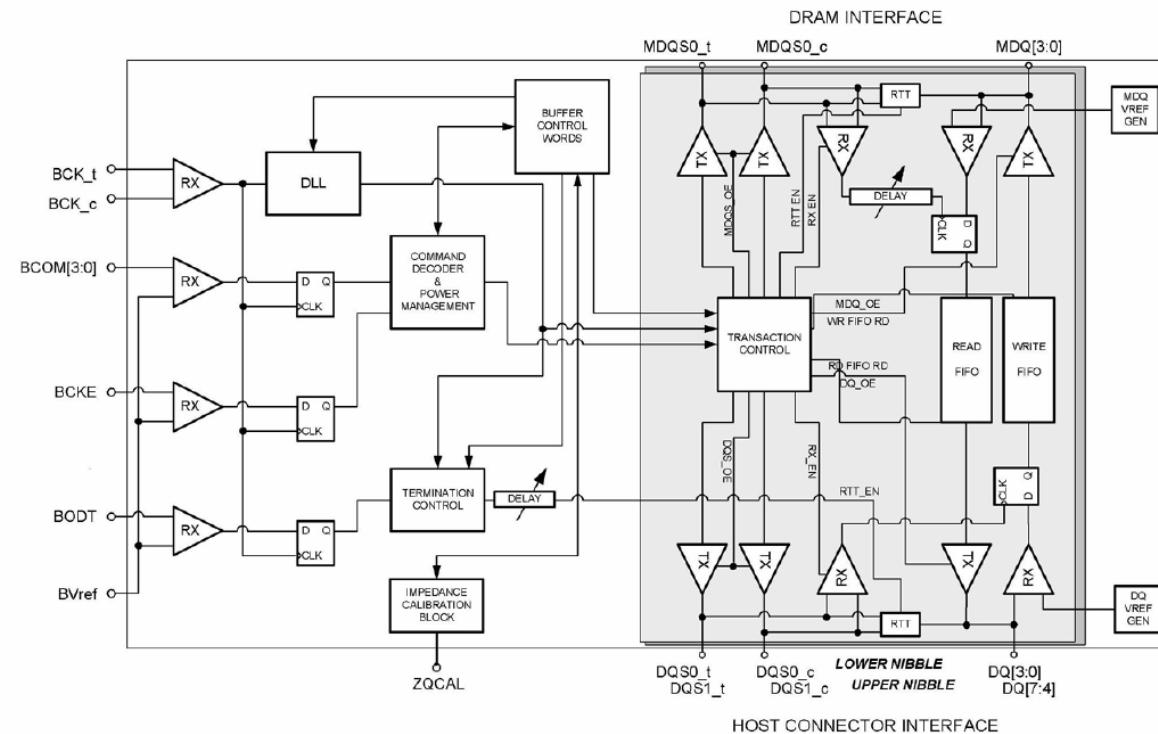
Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification (annotations added).

"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"

2.6 Logic Diagram

Figure 12 — Logic Diagram



See DDR4DB01 Standard

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

JEDEC DDR4 SDRAM Specification (annotations added).

See also SKH DDR4 Device Operation at 7.

"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus . If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data . Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

JEDEC DDR4 SDRAM Specification (annotations added).

See also SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 7.

The connector is also configured to provide electrical connections for address and control signals between the memory module and the system memory controller. For example, the SK hynix Products include the following input pins:

A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
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CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
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RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. These pins are multi-function. For example, for activation with ACT_n Low, the pins are Addresses A16, A15, and A14, but for non-activation commands with ACT_n High, these are Command pins for Read, Write, and other commands defined in the command truth table
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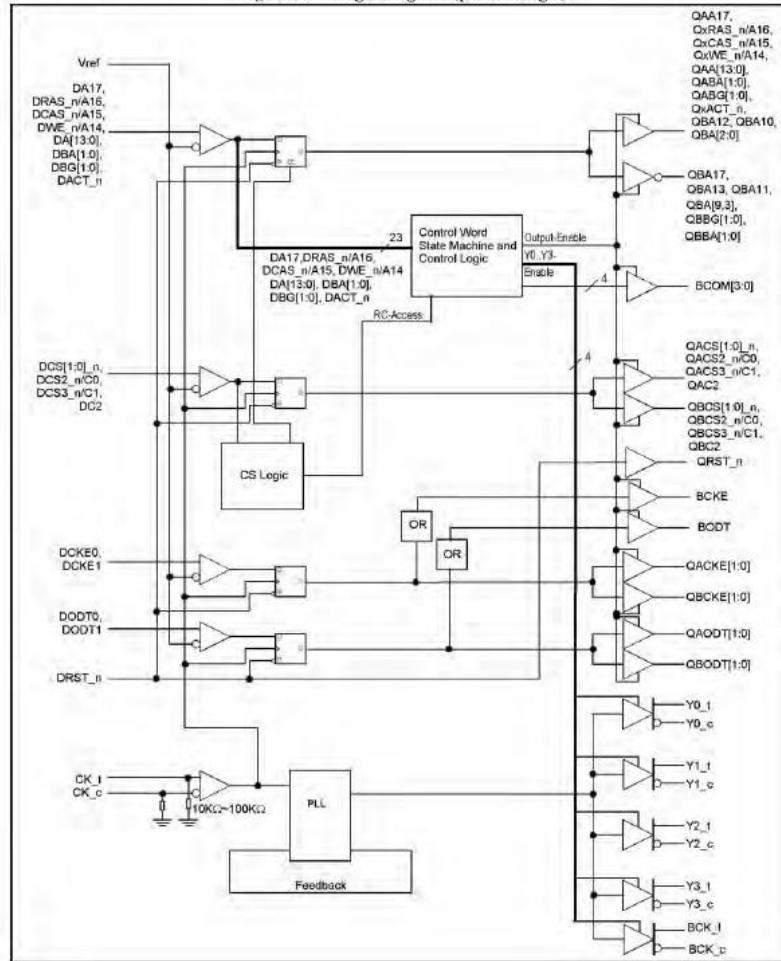
JEDEC LRDIMM Specification.

See also SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 6.

"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"

2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC0..DC1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal
Input Address and Command bus	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	
	DA14..DA16	CMOS ¹ V _{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function:
	DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
Clock inputs	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

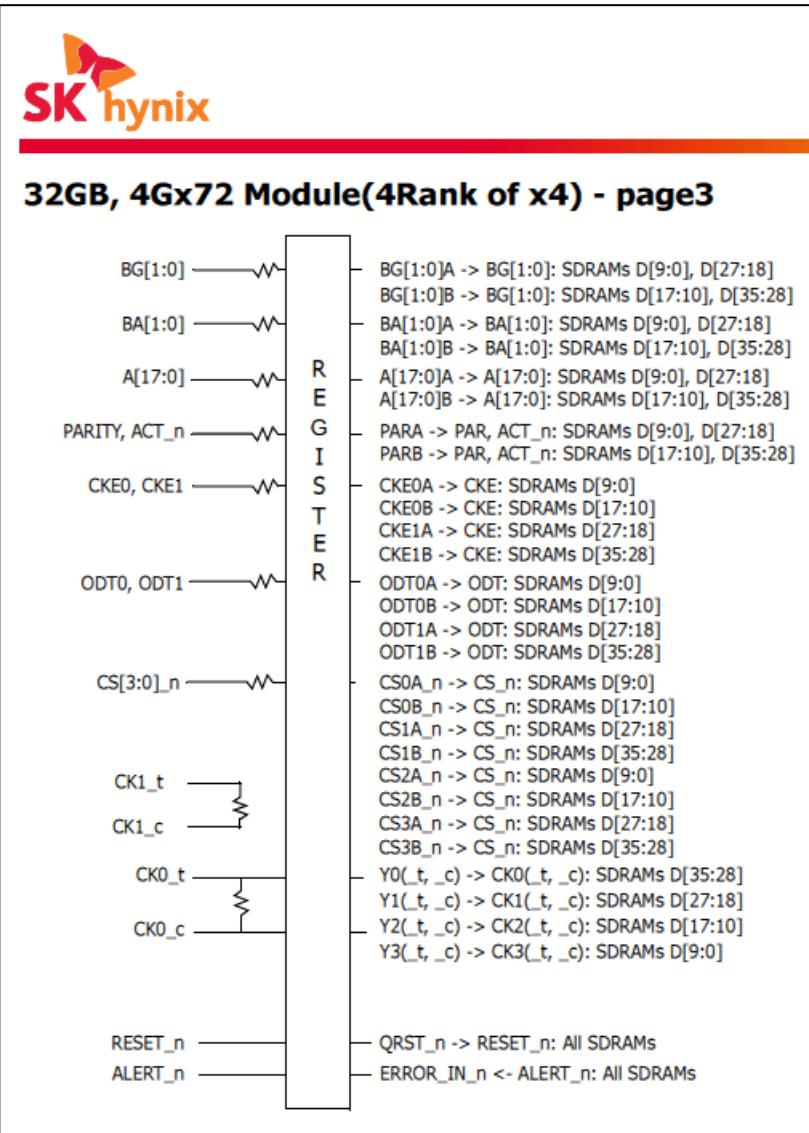
"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/I, QAODT0/I, QBCKE0/I, QBODT0/I	CMOS ²	Register output CKE and ODT signals.
	QACS0_n, QACSI_n, QBCS0_n, QBCSI_n	CMOS ²	Register output Chip Select signals.
	QACS2_n, QACSI_n, QBCS2_n, QBCSI_n or QAC0..QAC1, QBC0..QBC1	CMOS ²	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACI_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	VrefCA	V _{DD} ²	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"

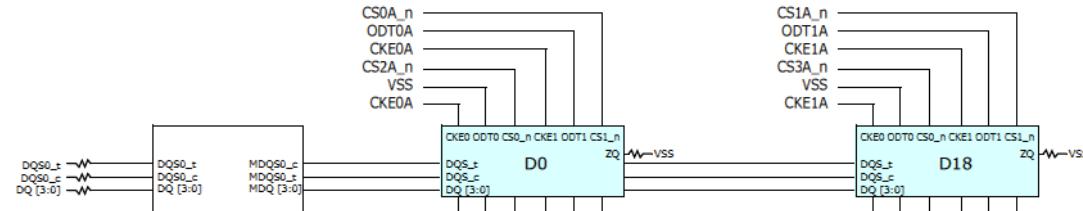


SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 16.

"a printed circuit board (PCB) having a connector configured to provide electrical connections for data, address and control signals between the memory module and the system memory controller;"



32GB, 4Gx72 Module(4Rank of x4) - page1



See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 14.

"memory devices mounted on the PCB and arranged in one or more ranks, each respective rank of the one or more ranks having a respective set of memory devices across a full bit-width of the memory module;"

memory devices mounted on the PCB and arranged in one or more ranks, each respective rank of the one or more ranks having a respective set of memory devices across a full bit-width of the memory module;

The SK hynix Products comprise memory devices mounted on the PCB and arranged in one or more ranks, each respective rank of the one or more ranks having a respective set of memory devices across a full bit-width of the memory module.

For example, the SK hynix Product includes a plurality of JEDEC-compliant synchronous dynamic random access memories ("SDRAMs").

JEDEC Standard No. 21C
Page 4.20.27-5

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, **Synchronous DRAM** Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.

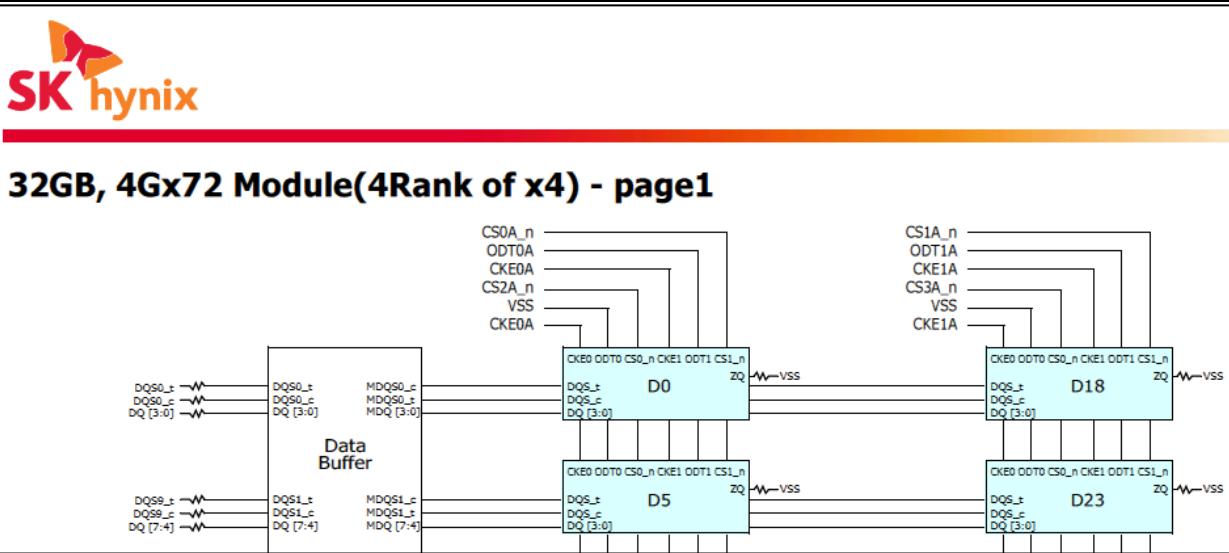
Reference design examples are included that provide an initial basis for DDR4 LRDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666, and PC4-3200 support. All DDR4 LRDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

An additional lower voltage of TBD is defined. PC4L is used to reference DIMMs capable of operation at this voltage level. The annex for each raw card will have specific entries to indicate DIMM operation at PC4 and PC4L voltage levels.

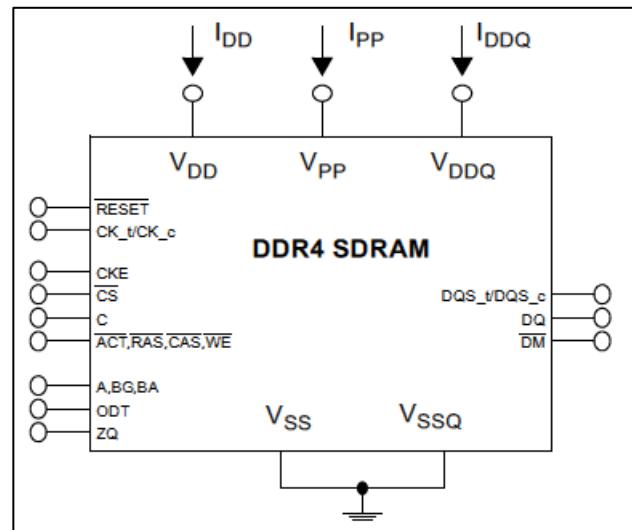
This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org).

See JEDEC LRDIMM Specification (annotations added).

"memory devices mounted on the PCB and arranged in one or more ranks, each respective rank of the one or more ranks having a respective set of memory devices across a full bit-width of the memory module;"



See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 14 (showing SDRAM devices D0, D18, D5, and D23).



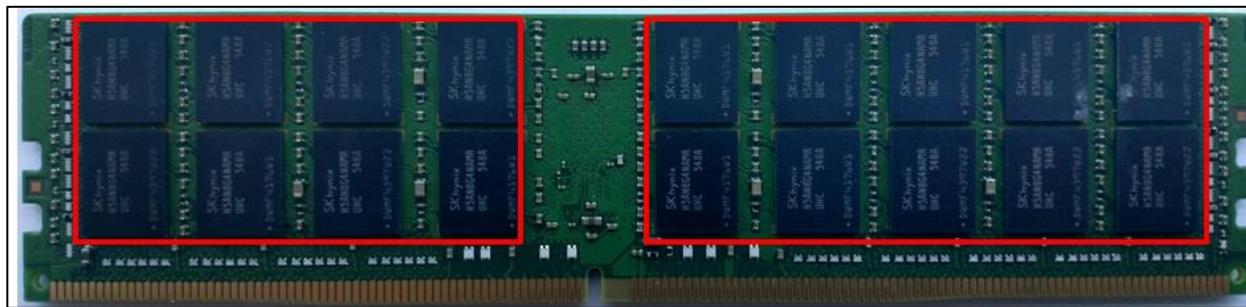
See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 51.

Specifically, the SK hynix HMA84GL7AMR4N-UHTE comprises 36 SDRAM components arranged in one or more ranks having a respective set of memory devices across a full bit-width of the memory module.

"memory devices mounted on the PCB and arranged in one or more ranks, each respective rank of the one or more ranks having a respective set of memory devices across a full bit-width of the memory module;"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE) (front side).



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE) (back side).



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE) (SDRAM).

The SDRAM devices are JEDEC compliant.

"memory devices mounted on the PCB and arranged in one or more ranks, each respective rank of the one or more ranks having a respective set of memory devices across a full bit-width of the memory module;"

**JEDEC
STANDARD**

DDR4 SDRAM

JESD79-4A

(Revision of JESD79-4, September 2012)

JEDEC DDR4 SDRAM Specification (annotations added).
See also SKH DDR4 Device Operation at 1.

The SDRAM devices are outlined in red in the figure below.

"memory devices mounted on the PCB and arranged in one or more ranks, each respective rank of the one or more ranks having a respective set of memory devices across a full bit-width of the memory module;"

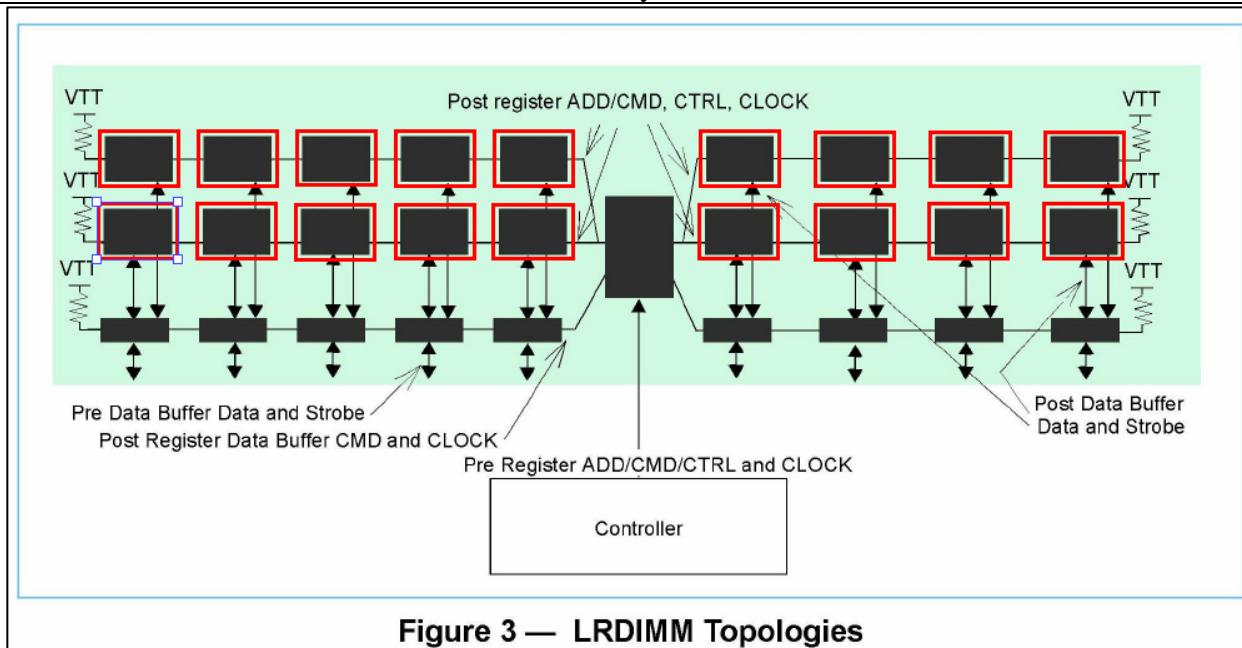


Figure 3 — LRDIMM Topologies

JEDEC LRDIMM Specification (annotation added).

See also SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 65.

Further, the SK hynix Product includes at least a first rank of SDRAM dies and a second rank of SDRAM dies. Each rank is comprised of x4 (4-bit) SDRAM dies that together send or receive 72 bits during a read or write operation.

Table 1 — DDR4 Product Family Attributes

DIMM Organization	x64, x72 ECC	Notes
DIMM Dimensions (nominal)	133.35 mm x 31.25 mm	Refer to MO-309
	133.35 mm x 18.75 mm	Refer to MO-309
Pin Count	288	
DDR4 SDRAMs Supported	4 Gb, 8 Gb, 16 Gb	78/106-ball FBGA package for x4 devices. Refer to MO-207: variations DT-z, DW-z
Capacity	16 GB, 32GB, 64 GB, 128 GB	
SDRAM width	x4	No designs using x8 SDRAMs currently planned.
Serial PD, Thermal Sensor (SPD-TSE)	512 byte	See EE1004-v and TSE2004av specifications
VDD, VDDQ, +5VSB, GND, TDI, TDO		

"memory devices mounted on the PCB and arranged in one or more ranks, each respective rank of the one or more ranks having a respective set of memory devices across a full bit-width of the memory module;"

See JEDEC LRDIMM Specification.

Ordering Information

Part Number	Density	Organization	Component Composition	# of ranks
HMA42GL7AFR4N-TF/UH	16GB	2Gx72	1Gx4(H5AN4G4NAFR)*36	2
HMA84GL7AMR4N-TF/UH	32GB	4Gx72	DDP 2Gx4(H5AN8G4NAMR)*36	4

See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

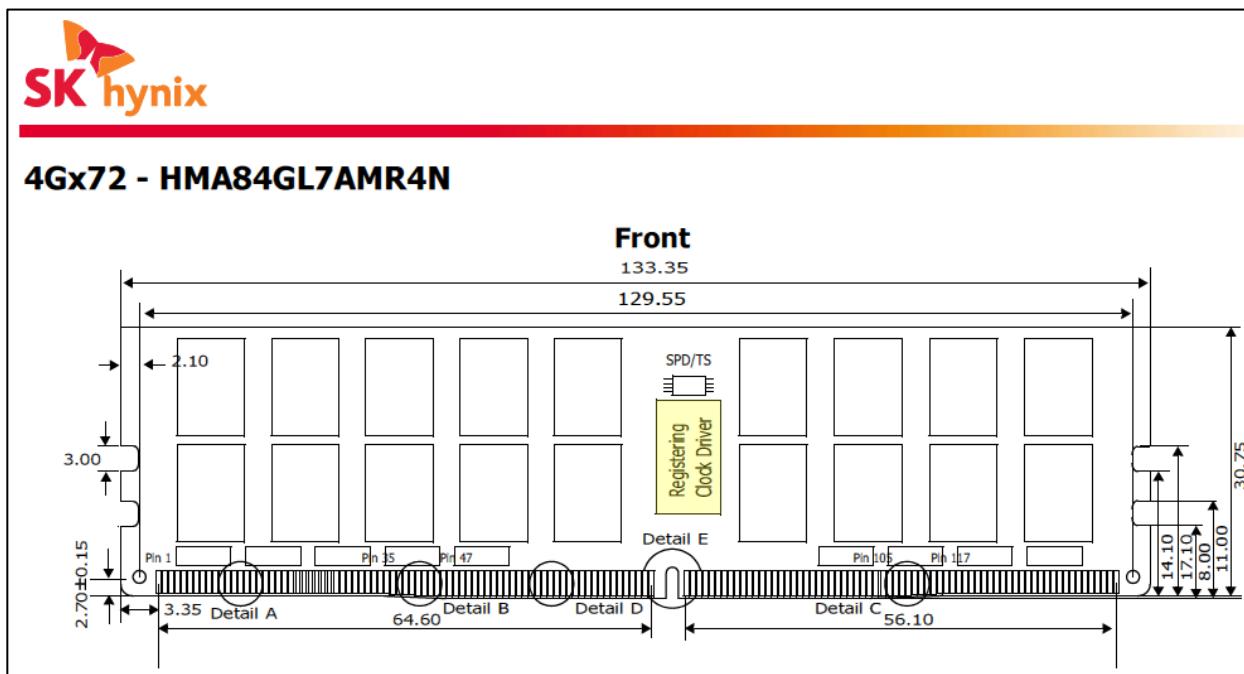
a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and

The SK hynix Products comprise a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector.

The SK hynix Products comprise a control module mounted on the PCB. For example, the SK hynix Products contain a JEDEC-compliant IDT 4RCD0124KC0 RCD on the printed circuit board.

Some modules have lower current requirements. Any specific module must meet the SDRAM, **DDR4RCD01**, and DDR4DB01 voltage requirements for its worst case supply currents.

See, e.g., JEDEC LRDIMM Specification (annotation added).



See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 65 (annotations added).

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE).

The IDT 4RCD0124KC0 RCD is JEDEC Compliant.

Features

- JEDEC Compliant RCD

See 4RCD0124K DDR4 Register Clock Driver Webpage at 1.

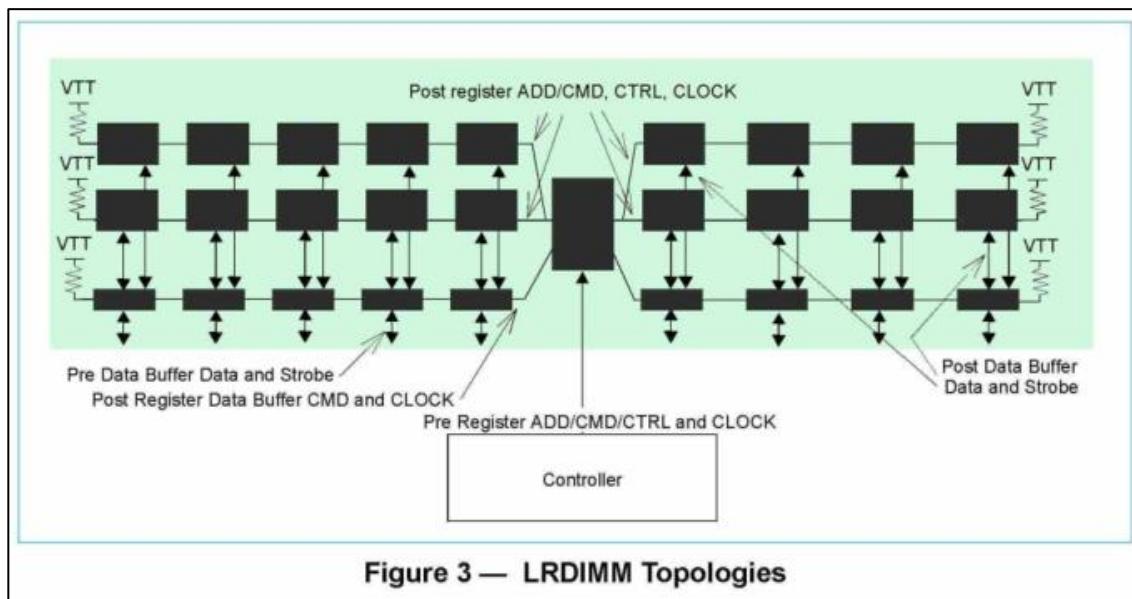
BENEFITS

- All devices are JEDEC® compliant and meet stringent requirements for reliability and application compliance

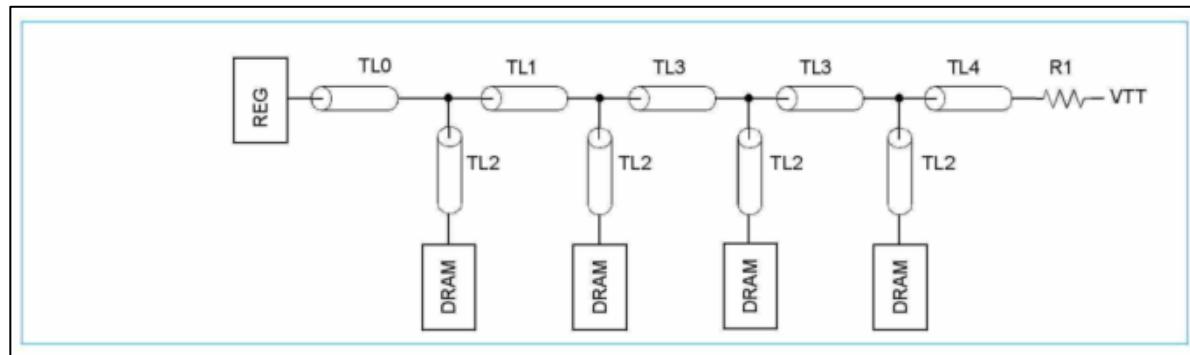
"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

IDT Leader in Server Memory Chipsets at 1.

The SK hynix Products comprise a control module electrically coupled to the connector and to the memory devices. For example, the IDT 4RCD0124KC0 RCD is coupled to the plurality of dynamic random access memory elements on the PCB.



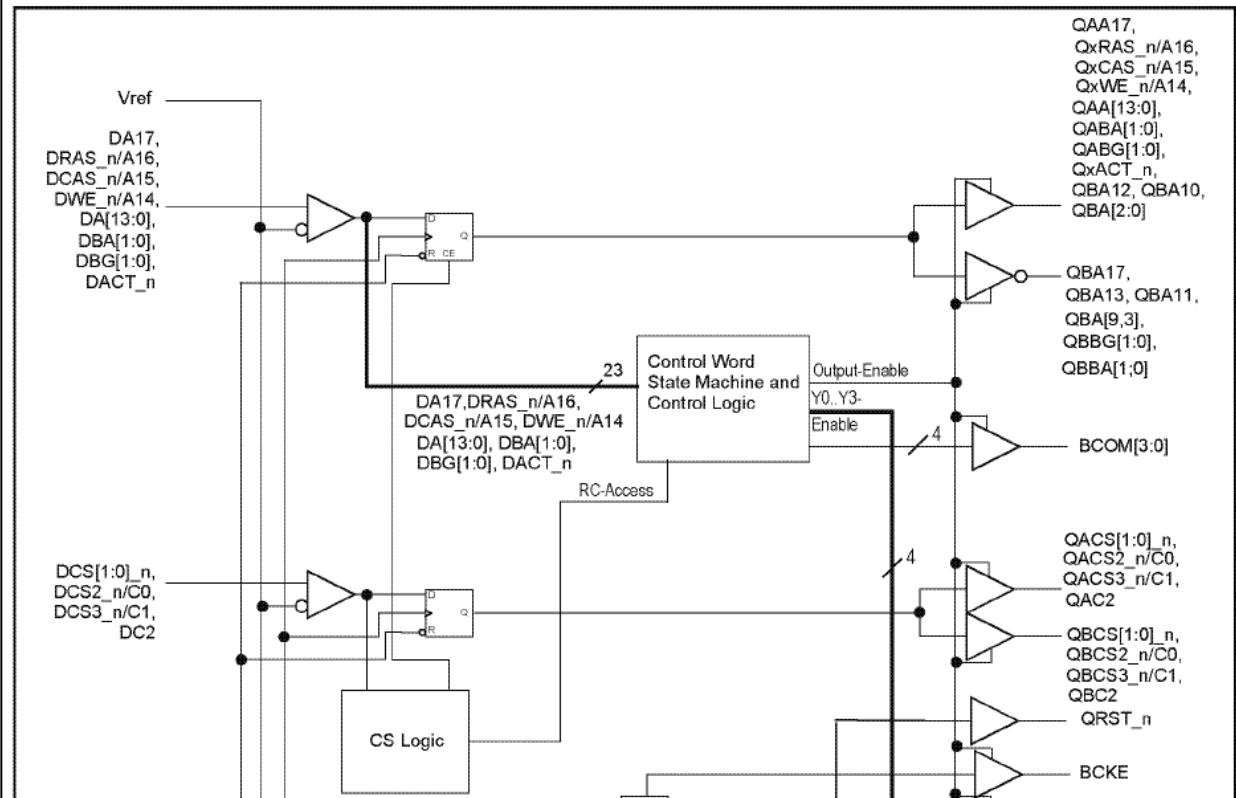
See JEDEC LRDIMM Specification.



See JEDEC LRDIMM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.17 Logic diagram



See JEDEC RCD01 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n or DC0..DC1	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
Input Address and Command bus	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal
	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
Clock inputs	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

See JEDEC RCD01 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

Table 16 — Terminal functions

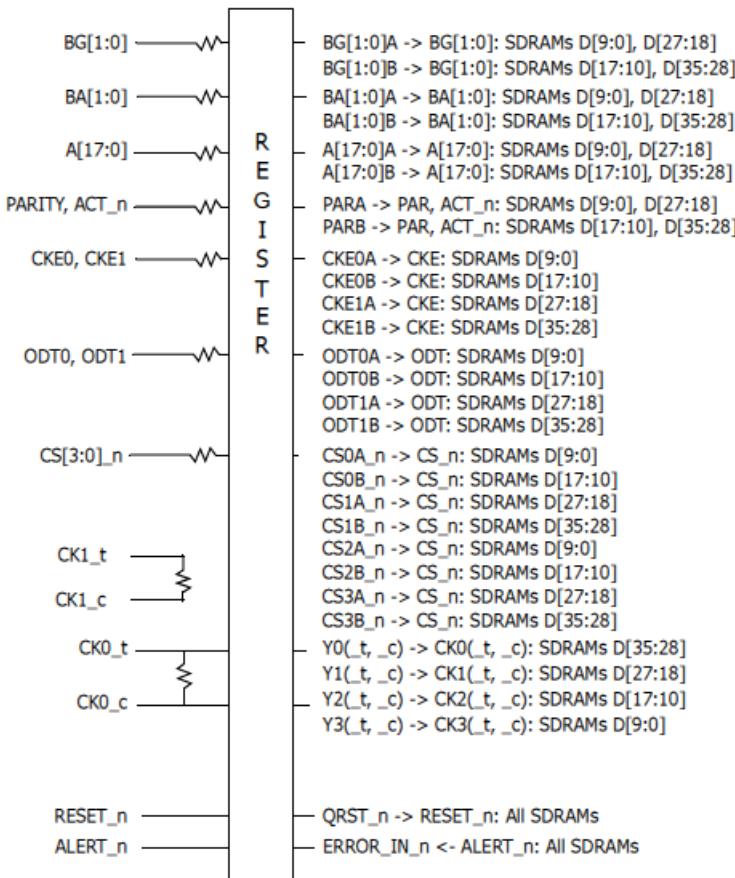
Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/I, QAODT0/I, QBCKE0/I, QBODT0/I QACS0_n, QACS1_n, QBCS0_n, QBCS1_n QACS2_n, QACS3_n, QBCS2_n, QBCS3_n or QAC0, QAC1, QBC0, QBC1	CMOS ²	Register output CKE and ODT signals. Register output Chip Select signals. Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QnCS2_n <=> QnC0 • QnCS3_n <=> QnC1
	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1 QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QnA14 <=> QnWE_n • QnA15 <=> QnCAS_n • QnA16 <=> QnRAS_n
	QAACT_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input

See JEDEC RCD01 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"



32GB, 4Gx72 Module(4Rank of x4) - page3

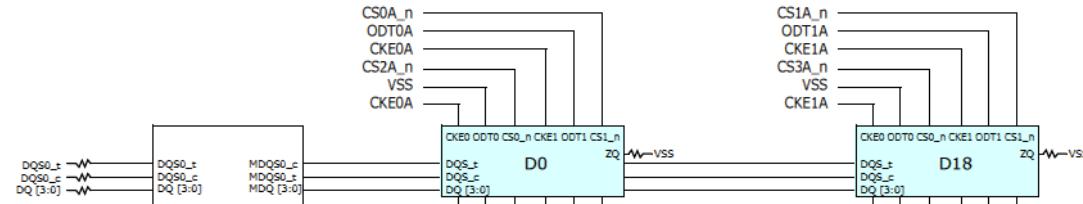


SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 16.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"



32GB, 4Gx72 Module(4Rank of x4) - page1



SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 14.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid]

Table 16 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A15	CAS_n /A15	WE_n /A14	BG0-BG1	BA0-BA1	C2-C0	A12/BC_n	A17/A15	A18/AP	Ad-AS	NOTE
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code		12		
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	V	L	V
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	V	H	V
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)		BG		BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	V	L	CA
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	V	H	CA
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	V	L	CA
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDSS	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	V	H	CA
Read with Auto Pre-charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Pre-charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	V	L	V

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t_NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set Commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .

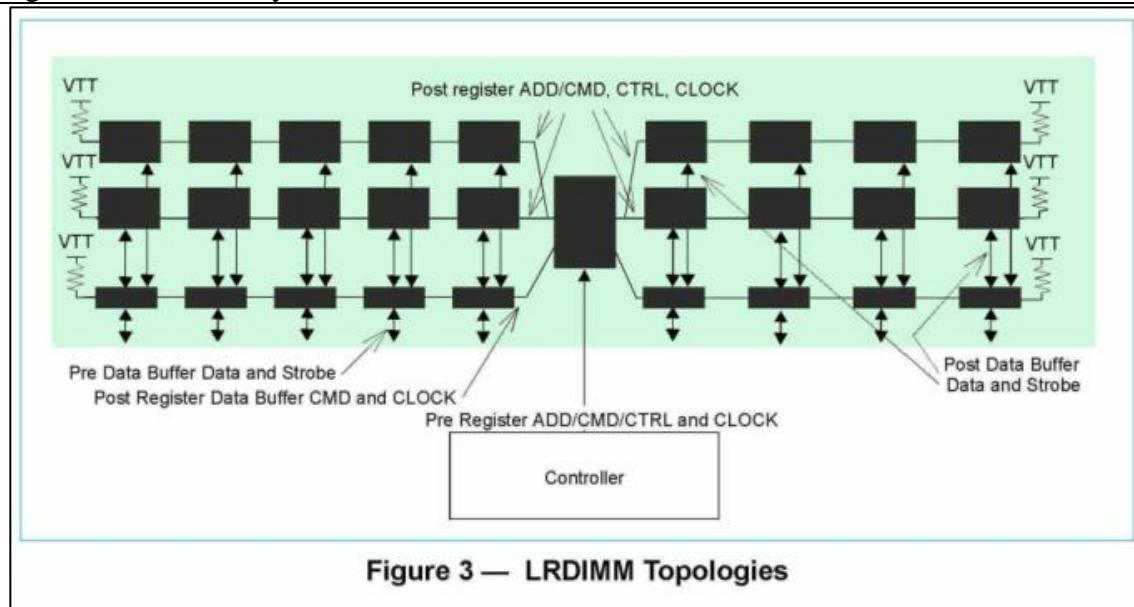
"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQLO-DQL7; DQSU corresponds to the data on DQ0-DQ7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DB/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
NOTE: Input only pins (BG0-BG1,BA0-BA1,A0-A17,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT, and RESET_n) do not supply termination.		

See JEDEC DDR4 DRAM Specification.

Further, the control module is coupled to the connector.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

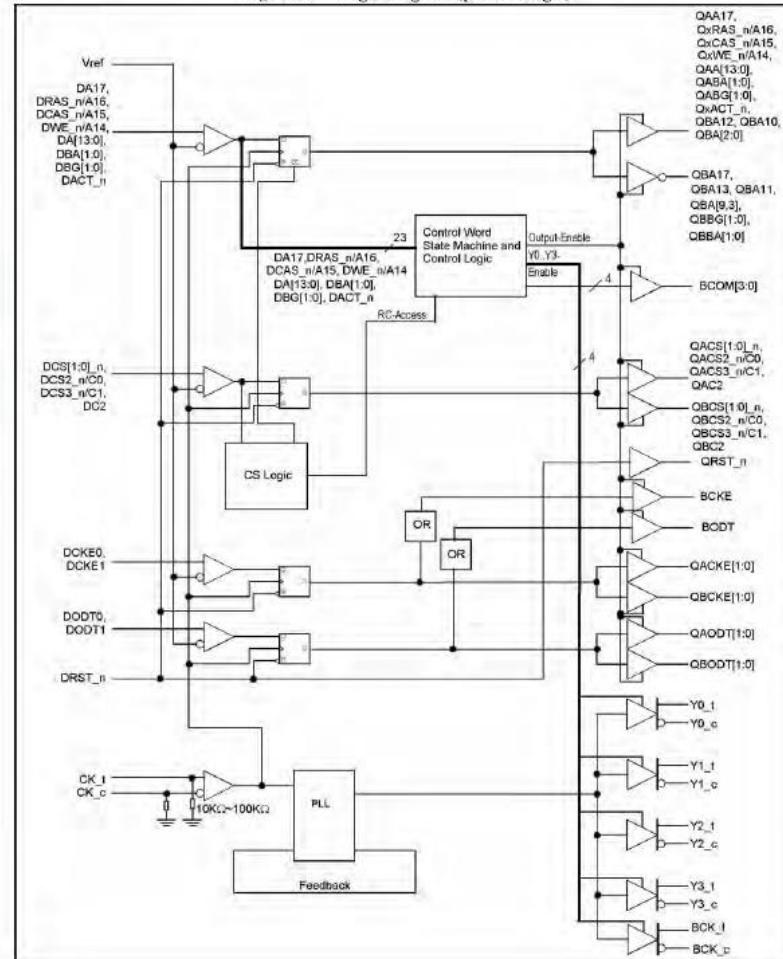


See JEDEC LRDIMM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

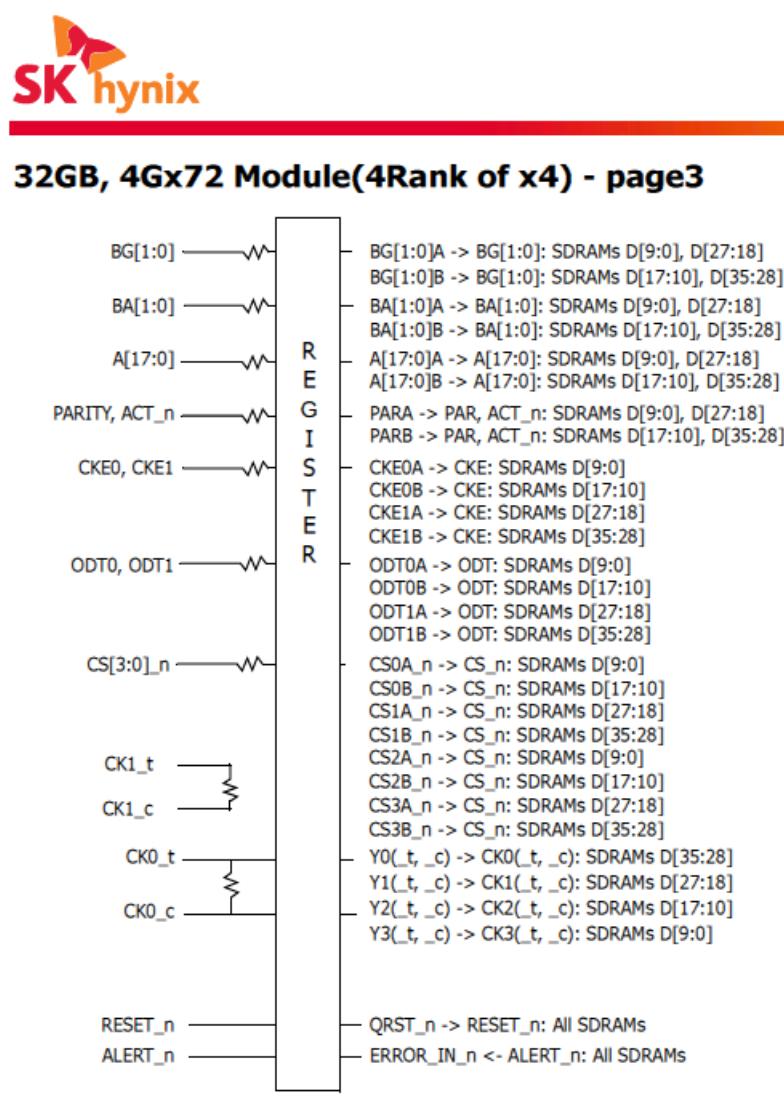
2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



See JEDEC DDR4 RCD01 Standard Rev 1.0.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"



See SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 16.

The SK hynix Products include a control module configured to output address and control signals to the memory devices based on information received via the connector. For example, the IDT RCD is configured to receive a set of input

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

address and control signals corresponding to a memory read or write command information (e.g., CS, A0-A17, ACT, RAS, CAS, WE, CKE, etc.) from the memory controller.

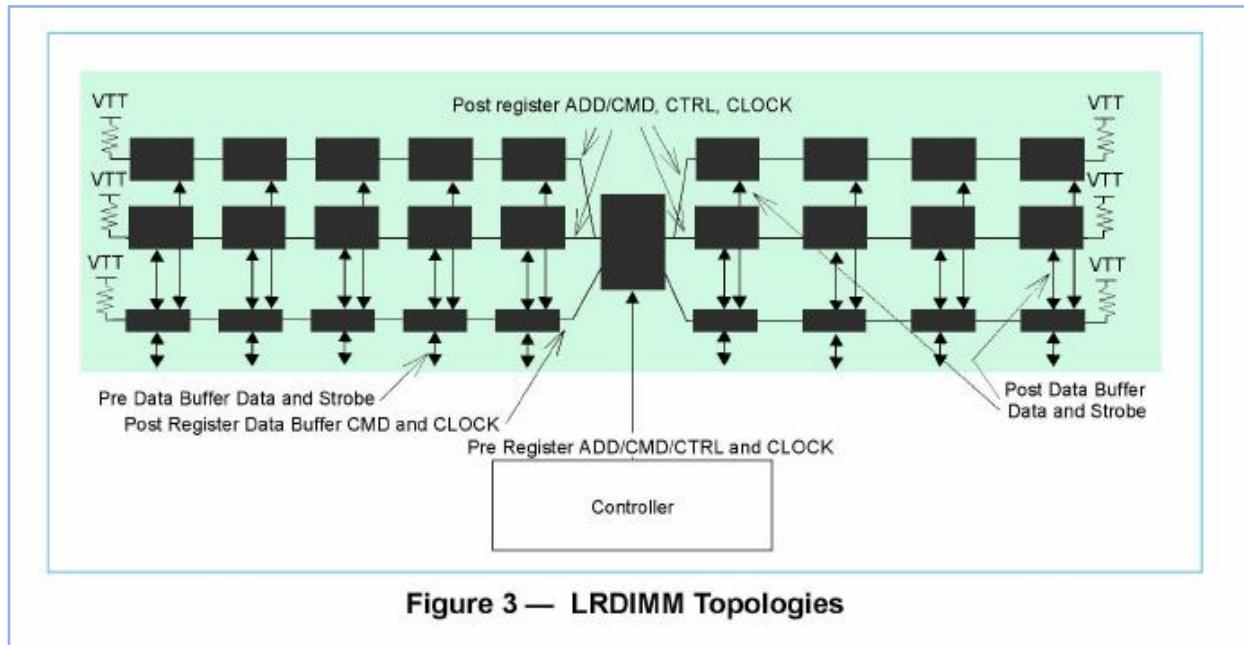


Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into seven groups. Figure 3 summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. The signal groups are:

1. DQ and DQS signals connector to Data Buffer (DB)
2. DQ and DQS signals DB to SDRAM
3. PreRegister ADD/CMD and CTRL
4. PreRegister CK
5. PostRegister ADD/CMD
6. PostRegister Control
7. PostRegister CK
8. PostRegister BCOM, BODT, BCKE
9. PostRegister BCK

The PreRegister ADD/CMD and CTRL group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, PARITY, CS_x_n, CKEx, and ODTx.

The PostRegister ADD/CMD group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, and PARITY.

The PostRegister CTRL group includes CS_x_n, CKEx, and ODTx.

See JEDEC LRDIMM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

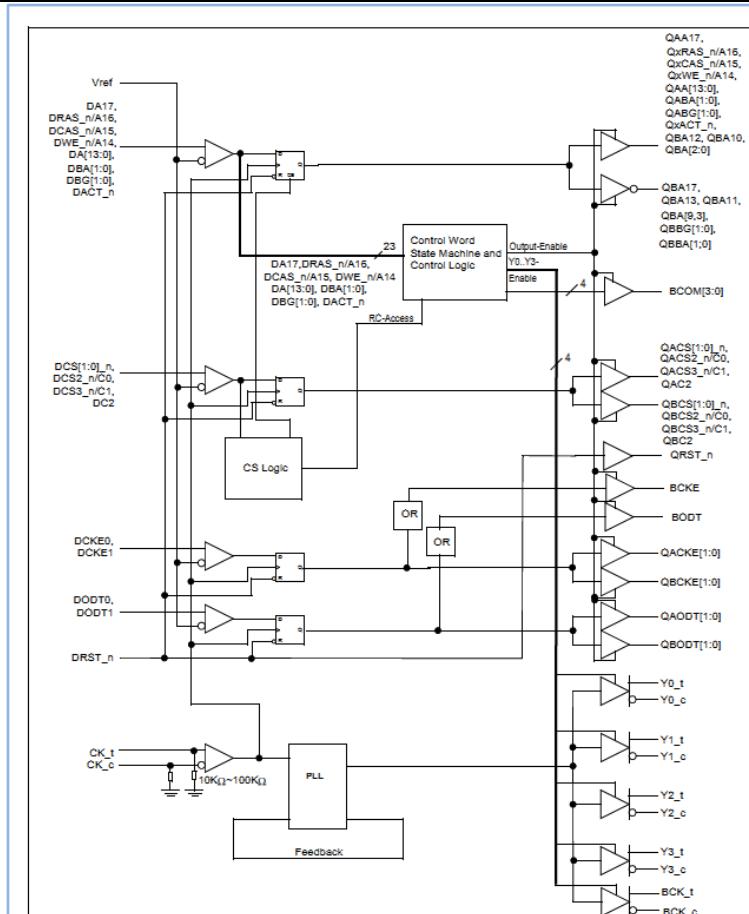
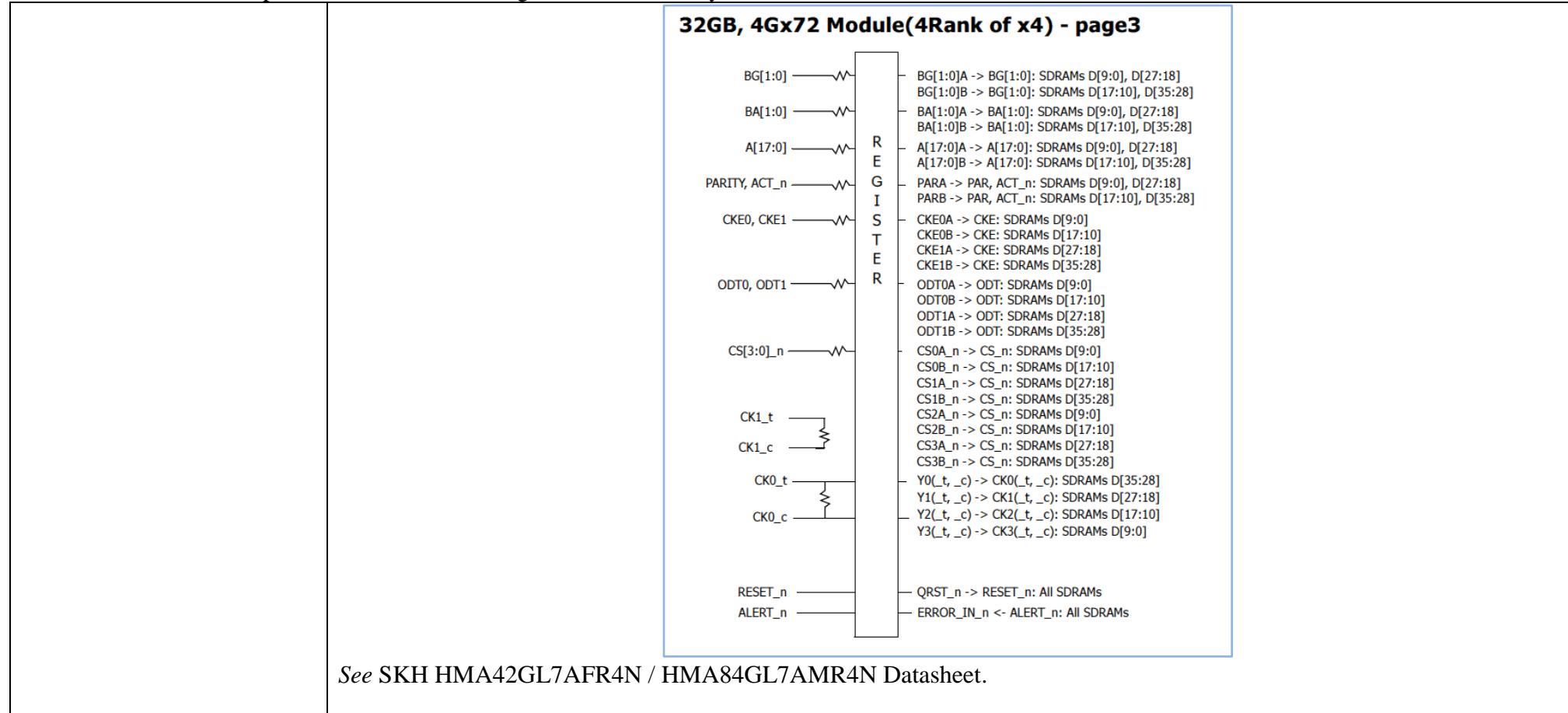


Figure 24 — Logic diagram (positive logic)

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"



"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

Table 4 — Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT, and CKE, are disabled during power-down. Input buffer, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. These pins are multi-function. For example, for activation with ACT_n Low, the pins are Addresses A16, A15, and A14, but for non-activation commands with ACT_n High, these are Command pins for Read, Write, and other commands defined in the command truth table
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped). See command truth table for details.

See JEDEC LRDIMM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid]

Table 16 — Command Truth Table

Function	Abbreviation	CKE				CS_n	ACT_n	RA_n	RA16	CAS_n	WE_n	RA16	BG0-BG1	BA0-BA1	C2-C9	A12/A13, A11	A10/AP	A0-A9	NOTE	
Mode Register Set	MRS	H H L L				H	H	L	L	L	H	L	BG	BA	V	OP Code				12
Refresh	REF	H H L L				H	H	L	L	L	H	L	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H L L L				H	H	L	L	L	H	L	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L H L L				H	X	X	X	X	X	X	V	V	X	X	X	X	X	7,8,9,10
Single Bank Precharge	PRE	H H L H				L	H	L	H	L	BG	BA	V	V	V	V	L	V		
Precharge all Banks	PREA	H H L H				L	H	L	H	L	V	V	V	V	V	V	V	H	V	
RFU	RFU	H H L H				L	H	L	H	H	RFU									
Bank Activate	ACT	H H L L				Row Address (RA)				BG BA V				Row Address (RA)						
Write (Fixed BL8 or BC4)	WR	H H L H				H	H	L	H	L	BG	BA	V	V	V	V	L	CA		
Write (BC4, on the Fly)	WR54	H H L H				H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WR58	H H L H				H	H	L	H	H	L	L	BG	BA	V	V	H	V	L	CA
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H H L H				H	H	L	H	H	L	L	BG	BA	V	V	V	V	H	CA
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H H L H				H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H H L H				H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H H L H				H	H	L	H	H	L	H	BG	BA	V	V	V	V	L	CA
Read (BC4, on the Fly)	RDS4	H H L H				H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H H L H				H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H H L H				H	H	L	H	H	L	H	BG	BA	V	V	V	V	H	CA
Read with Auto Pre-charge (BC4, on the Fly)	RDAS4	H H L H				H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Pre-charge (BL8, on the Fly)	RDAS8	H H L H				H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H H L H				H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H H H X				H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H L H X				H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L H H X				L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H H L H H L				H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H H L H H L				H	H	L	H	H	H	L	V	V	V	V	V	L	V	

NOTE 1: All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RA_n, RA16, CAS_n, WE_n, and CKE at the rising edge of the clock. The MRS has CKE, RA, and CKE as inputs.

See JEDEC DDR4 DRAM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n or DC0..DC1	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
Input Address and Command bus	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal
	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
Clock inputs	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

See JEDEC RCD01 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/I, QAODT0/I, QBCKE0/I, QBODT0/I QACS0_n, QACS1_n, QBCS0_n, QBCS1_n QACS2_n, QACS3_n, QBCS2_n, QBCS3_n or QAC0, QAC1, QBC0, QBC1	CMOS ²	Register output CKE and ODT signals. Register output Chip Select signals. Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QnCS2_n <=> QnC0 • QnCS3_n <=> QnC1
	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1 QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QnA14 <=> QnWE_n • QnA15 <=> QnCAS_n • QnA16 <=> QnRAS_n
	QAACT_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input

See JEDEC RCD01 Specification.

The IDT RCD outputs memory address and control signals (e.g., as part of read and write commands) to the memory devices according to the system address and control signals.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into seven groups. Figure 3 summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. The signal groups are:

1. DQ and DQS signals connector to Data Buffer (DB)
2. DQ and DQS signals DB to SDRAM
3. PreRegister ADD/CMD and CTRL
4. PreRegister CK
5. PostRegister ADD/CMD
6. PostRegister Control
7. PostRegister CK
8. PostRegister BCOM, BODT, BCKE
9. PostRegister BCK

The PreRegister ADD/CMD and CTRL group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, PARITY, CSx_n, CKEx, and ODTx.

The PostRegister ADD/CMD group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, and PARITY.

The PostRegister CTRL group includes CSx_n, CKEx, and ODTx.

See JEDEC LRDIMM Specification.

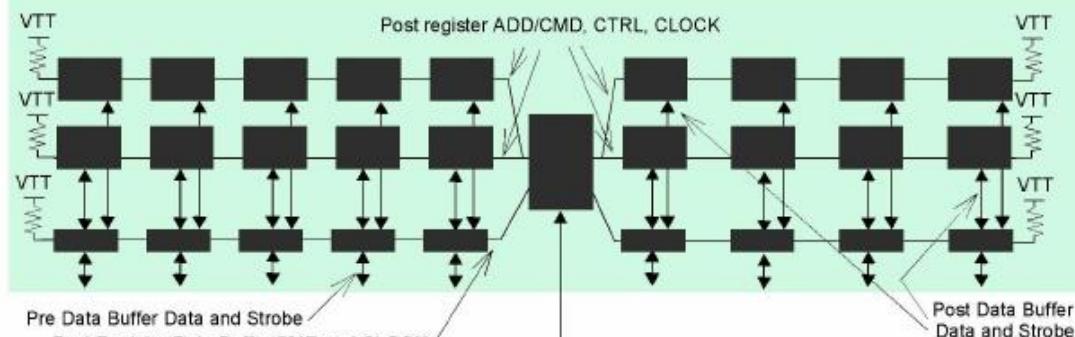


Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

Table 4 — Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge, Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT, and CKE, are disabled during power-down. Input buffer, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. These pins are multi-function. For example, for activation with ACT_n Low, the pins are Addresses A16, A15, and A14, but for non-activation commands with ACT_n High, these are Command pins for Read, Write, and other commands defined in the command truth table
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped). See command truth table for details.

See JEDEC LRDIMM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

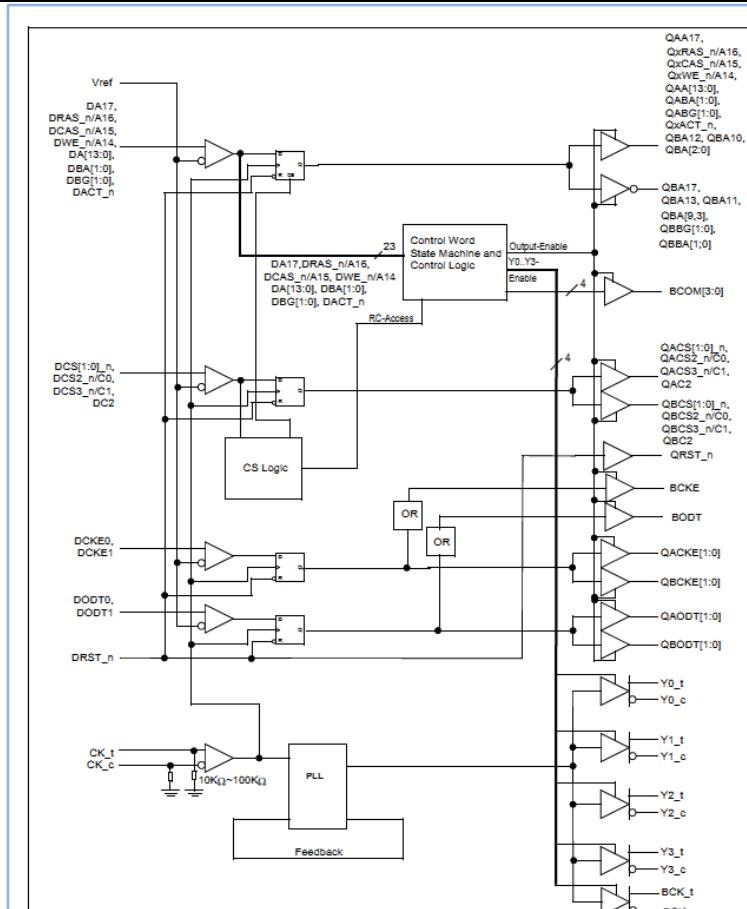
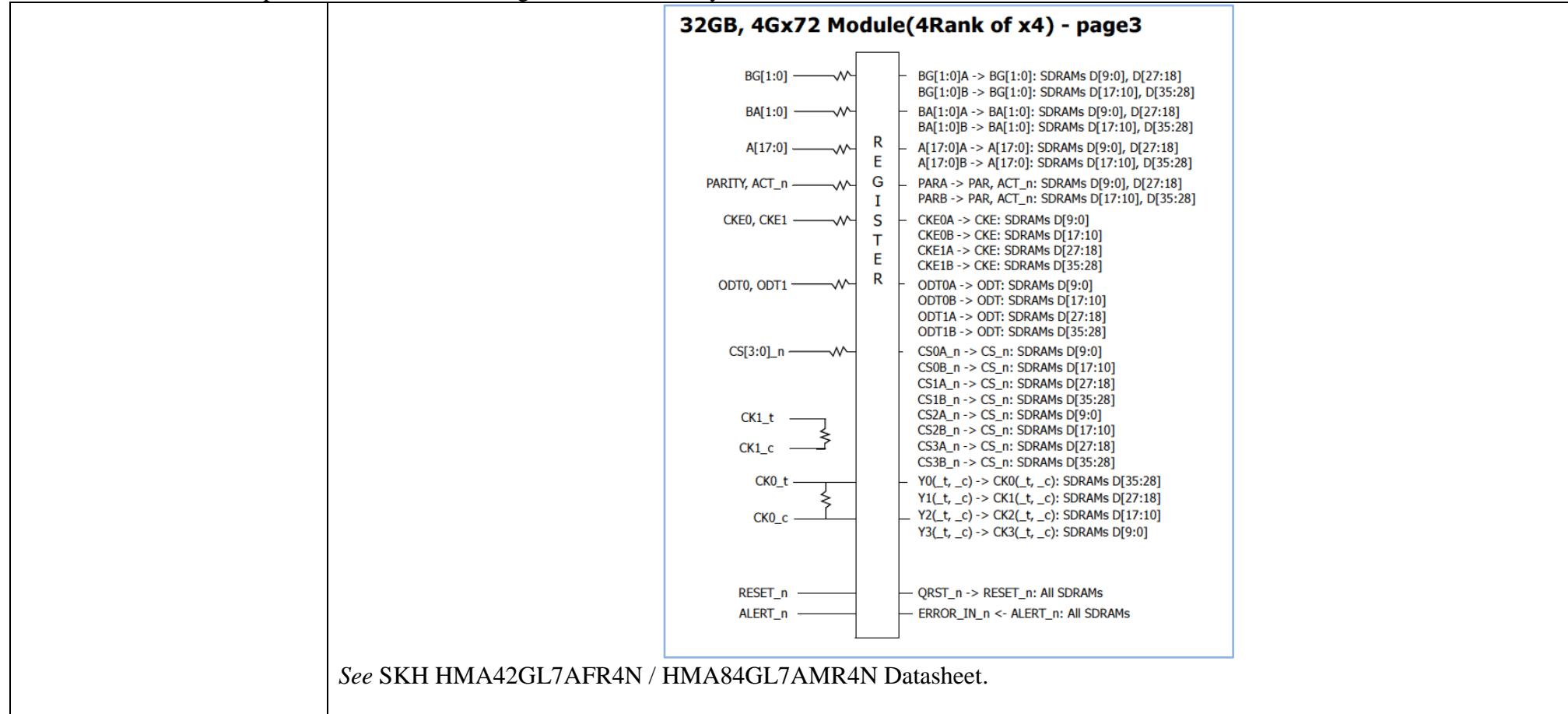


Figure 24 — Logic diagram (positive logic)

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"



"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC0..DC1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal
Input Address and Command bus	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	
	DA14..DA16	CMOS ¹ V _{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function:
	DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
Clock inputs	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

See JEDEC RCD01 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/I, QAODT0/I, QBCKE0/I, QBODT0/I QACS0_n, QACS1_n, QBCS0_n, QBCS1_n QACS2_n, QACS3_n, QBCS2_n, QBCS3_n or QAC0, QAC1, QBC0, QBC1	CMOS ²	Register output CKE and ODT signals. Register output Chip Select signals. Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QnCS2_n <=> QnC0 • QnCS3_n <=> QnC1
	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1 QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QnA14 <=> QnWE_n • QnA15 <=> QnCAS_n • QnA16 <=> QnRAS_n
	QAACT_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input

See JEDEC RCD01 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 16 — Command Truth Table

Function	Abbreviation	CKE Previous Cycle	CKE Current Cycle	CS_n	ACT_n	RAS_n IA16	CAS_n IA15	WE_n IA14	BG0- BG1	BA0- BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE	
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V					OP Code	12
Refresh	REF	H	H	L	H	L	H	V	V	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	H	V	V	V	V	V	V	V	V		7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H								RFU	
Bank Activate	ACT	H	H	L	L				Row Address (RA)			Row Address (RA)					
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA		
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA		
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	V	H	CA	
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA		
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA		
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA		
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA		
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA		
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	V	H	CA	
Read with Auto Pre-charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA		
Read with Auto Pre-charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA		
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V		
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V		

NOTE 1: ALL DDR4 SDRAM commands are defined in terms of CKE = ACT = CAS = RAS = WE = VREF = VREF + VREF and CYC at the rising edge of the clock. The 16B = 12C =

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set Commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQLO-DQL7; DQSU corresponds to the data on DQLO-DQH7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DB/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
NOTE: Input only pins (BG0-BG1,BA0-BA1,A0-A17,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT, and RESET_n) do not supply termination.		

See JEDEC DDR4 DRAM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.4 DDR4 SDRAM X4/8 Ballout using MO-207									
	1	2	3	4	5	6	7	8	9
A	VDD	VSSQ	TDQS_c ³				DM_n, DBI_n TDQS_t ² , (NC) ¹	VSSQ	VSS
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ
D	VSSQ	DQ4 (NC) ¹	DQ2				DQ3	DQ5 (NC) ¹	VSSQ
E	VSS	VDDQ	DQ6 (NC) ¹				DQ7 (NC) ¹	VDDQ	VSS
F	VDD	(C2) ⁵ ODT1 ⁶	ODT				CK_t	CK_c	VDD
G	VSS	(C0) ⁵ CKE1 ⁶	CKE				CS_n	(C1) ⁵ (CS1_n) ⁶	TEN (NC) ⁷
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD
K	VSS	BA0	A4				A3	BA1	VSS
L	RESET_n	A6	A0				A1	A5 ALERT_n	A9
M	VDD	A8	A2					VPP	A17 (NC) ⁴
N	VSS	A11	PAR						A13

NOTE 1 These pins are not connected for the X4 configuration.
 NOTE 2 TDQS_t is not valid for the x4 configuration.
 NOTE 3 TDQS_c is not valid for the x4 configuration.
 NOTE 4 A17 is only defined for the x4 configuration.
 NOTE 5 These pins are for stacked component such as 3D8. For mono package, these pins are NC.
 NOTE 6 ODT1 / CKE1 / CS1_n are used together only for DDP.
 NOTE 7 TEN is optional for 8Gb and above. This pin is not connected if TEN is not supported.

Figure 1 — DDR4 Ball Assignments for the x4/8 component

See JEDEC DDR4 SDRAM Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.2 Features and Functions

The DDR4RCD01 has three basic modes of operation associated with the DA[1:0] bits in the DIMM Configuration Control Word (RC0D):

- In **Direct DualCS mode** (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. The inputs pins DC[2:0] are forwarded to two sets of output pins, QAC[2:0] and QBC[2:0]. This is the normal operating mode ("QuadCS disabled" and "Encoded CS disabled").
- In **Direct QuadCS mode** (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "QuadCS enabled" mode.
- In **Encoded QuadCS mode** (DA[1:0] = 11), two copies of four output chip selects, i.e., QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "Encoded QuadCS" mode.

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.9 Output Inversion Enabling/Disabling

Output Inversion is enabled by default, after DRST_n is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs. The DDR4 register output signals are divided into two classes: signals that can be inverted (e.g., regular addresses) and signals that cannot be inverted (because they have a special function), see [Figure 18](#). Only the following 14 signals in the first class will be driven to the complement of the matching A-outputs: QBA3 to QBA9, QBA11, QBA13, QBA17, QBA0 to QBBA1 and QBBG0 to QBBG1.

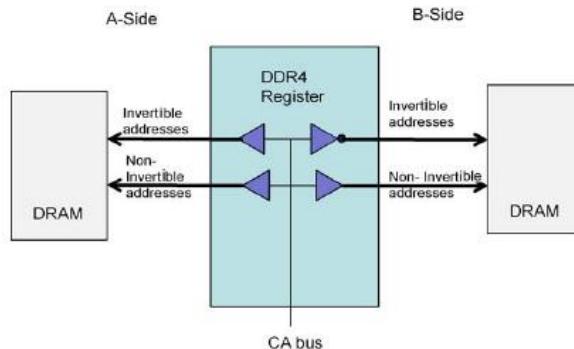


Figure 18 — Output Inversion Functional Diagram.

The Output Inversion feature is always enabled, even during DRAM MRS commands. In order to ensure that the DRAM receives the correct (i.e., uninverted) MRS bits, the host-to-register-to-DRAM MRS programming is split into a two-step process, see [Figure 19](#). In the first step the A-side DRAMs are programmed using non-inverted addresses from the host. In the second step the B-side DRAMs are programmed using inverted addresses for the invertible address signals and non-inverted addresses for the non-invertible address signals from the host.

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

"a control module mounted on the PCB and electrically coupled to the connector and to the memory devices, wherein the control module is configured to output address and control signals to the memory devices based on information received via the connector; and"

2.11 Latency Equalization Support

3D Stacked SDRAMs have a higher CAS latency than monolithic devices. For greater platform flexibility it is highly desirable to mix DIMMs with both 3DS and mono SDRAMs on the same DDR4 channel. Since memory controllers typically can only handle devices with equal CAS latencies in the same channel, it is required that the DDR4 register has a mechanism to increase the CAS latency of mono SDRAMs to match the CAS latency of 3DS SDRAMs. However, this mechanism only equalizes the DRAM latencies, not the total DIMM latencies. Hence this DDR4 register mechanism does not by itself allow mixing DDR4 RDIMMs and DDR4 LRDIMMs in the same channel.

To equalize different SDRAM latencies, the DDR4 register supports a programmable latency adder of 0 nCK, 1nCK, 2nCK, 3nCK or 4nCK for all DRAM commands, see conceptual diagram in Figure 2.12. The power-up default is 1nCK latency adder.

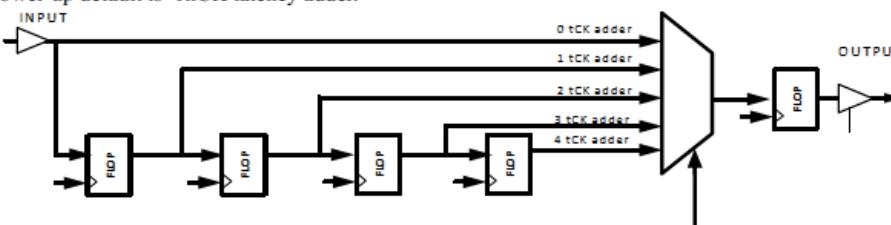


Figure 21 — Latency Equalizer Delays

See JEDEC RCD01 Specification.

See JEDEC RCD02 Specification.

2.5.2 Control Bus Timing

The output signals BCOM, BODT and BCKE are driven at the same time as the QxCA outputs, i.e., they are affected by the Command Latency Adder Control Word RC0F but a latency adder of 0 is not a valid configuration. For speeds above 2400MT/s, a minimum latency adder of 2 nCK is required in RC0F.

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

"a plurality of data handlers mounted on the PCB, wherein each respective data handler of the plurality of data handlers includes a data handler logic element, wherein each respective data handler of the plurality of data handlers is electrically coupled between a respective group of one or more memory devices and the connector, the respective group of one or more memory devices including at least one respective memory device in each of the one or more ranks;"

a plurality of data handlers mounted on the PCB, wherein each respective data handler of the plurality of data handlers includes a data handler logic element, wherein each respective data handler of the plurality of data handlers is electrically coupled between a respective group of one or more memory devices and the connector, the respective group of one or more memory devices including at least one respective memory device in each of the one or more ranks;

The SK hynix Products comprise a plurality of data handlers mounted on the PCB, wherein each respective data handler of the plurality of data handlers includes a data handler logic element, wherein each respective data handler of the plurality of data handlers is electrically coupled between a respective group of one or more memory devices and the connector, the respective group of one or more memory devices including at least one respective memory device in each of the one or more ranks.

The SK hynix Products include a circuit that comprises a plurality of data handlers mounted on the PCB. For example, the SK Hynix Products include a plurality of IDT 4DB0226KA3AVG8 Data Buffers.

The below picture of the SK Hynix HMA84GL7AMR4N-TFTE AB DIMM is representative of the SK Hynix LRDIMM Products and the data buffers they include.

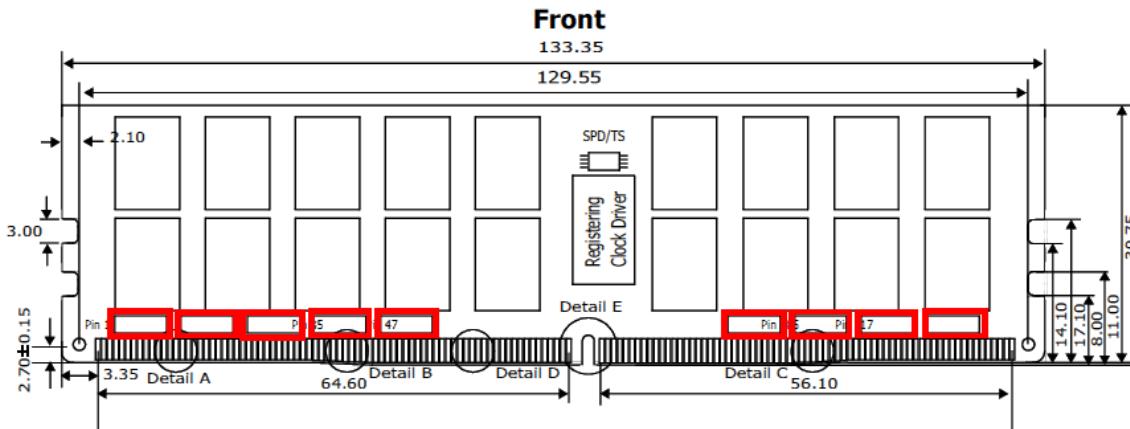


(Exemplary Photo of SK Hynix HMA84GL7AMR4N-TFTE AB).

"a plurality of data handlers mounted on the PCB, wherein each respective data handler of the plurality of data handlers includes a data handler logic element, wherein each respective data handler of the plurality of data handlers is electrically coupled between a respective group of one or more memory devices and the connector, the respective group of one or more memory devices including at least one respective memory device in each of the one or more ranks;"



4Gx72 - HMA84GL7AMR4N



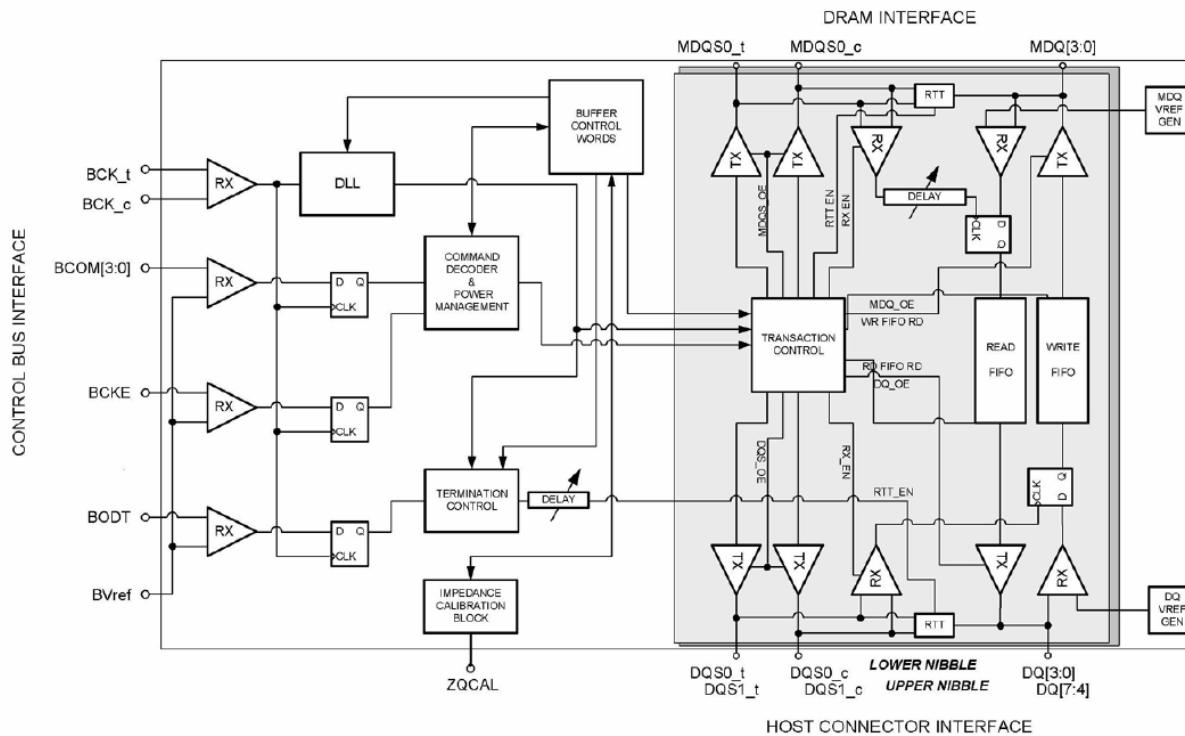
See HMA84GL7AMR4N Datasheet.

Each respective data handler of the plurality of data handlers includes a data handler logic element.

"a plurality of data handlers mounted on the PCB, wherein each respective data handler of the plurality of data handlers includes a data handler logic element, wherein each respective data handler of the plurality of data handlers is electrically coupled between a respective group of one or more memory devices and the connector, the respective group of one or more memory devices including at least one respective memory device in each of the one or more ranks;"

2.6 Logic Diagram

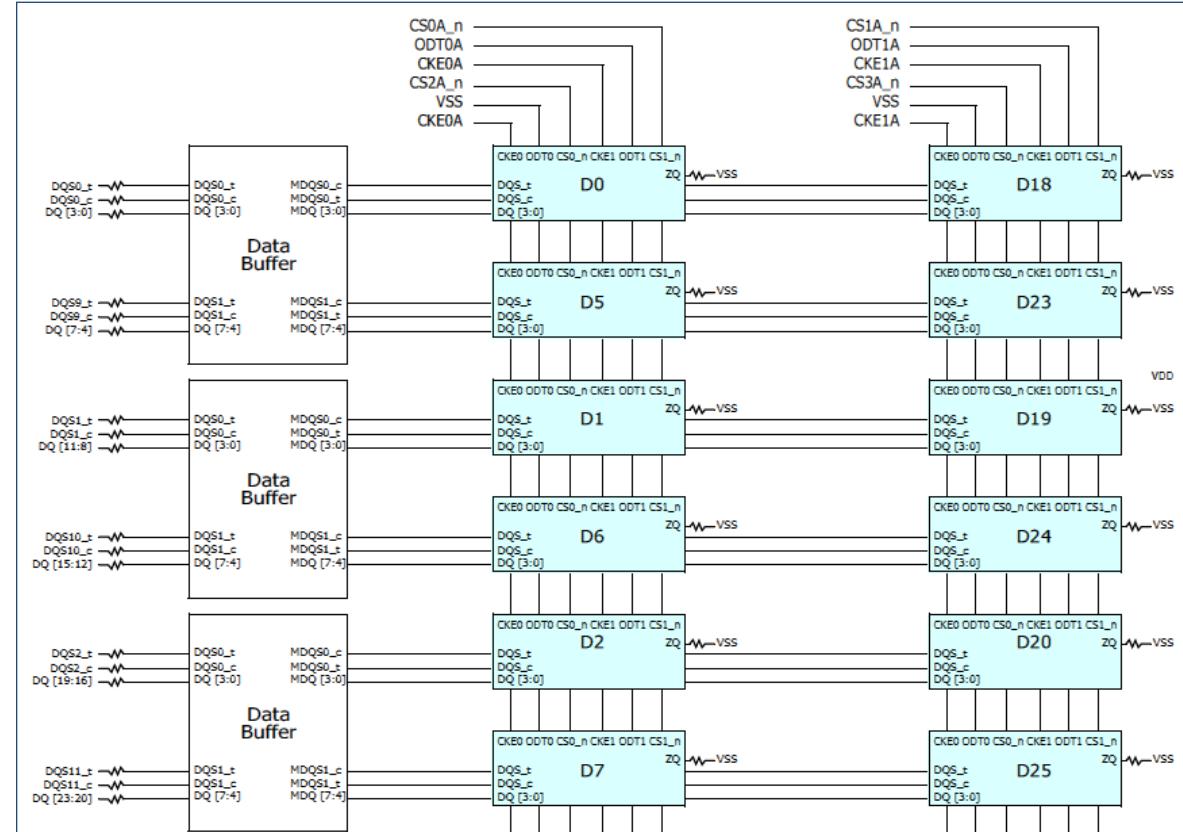
Figure 12 — Logic Diagram



See DDR4DB01 Standard

Each respective data handler of the plurality of data handlers is electrically coupled between a respective group of one or more memory devices and the connector, the respective group of one or more memory devices including at least one respective memory device in each of the one or more ranks. For example, the plurality of data buffers are coupled to corresponding DDR4 SDRAM memory devices and a connector.

"a plurality of data handlers mounted on the PCB, wherein each respective data handler of the plurality of data handlers includes a data handler logic element, wherein each respective data handler of the plurality of data handlers is electrically coupled between a respective group of one or more memory devices and the connector, the respective group of one or more memory devices including at least one respective memory device in each of the one or more ranks;"



See HMA84GL7AMR4N Datasheet

2.1 Description

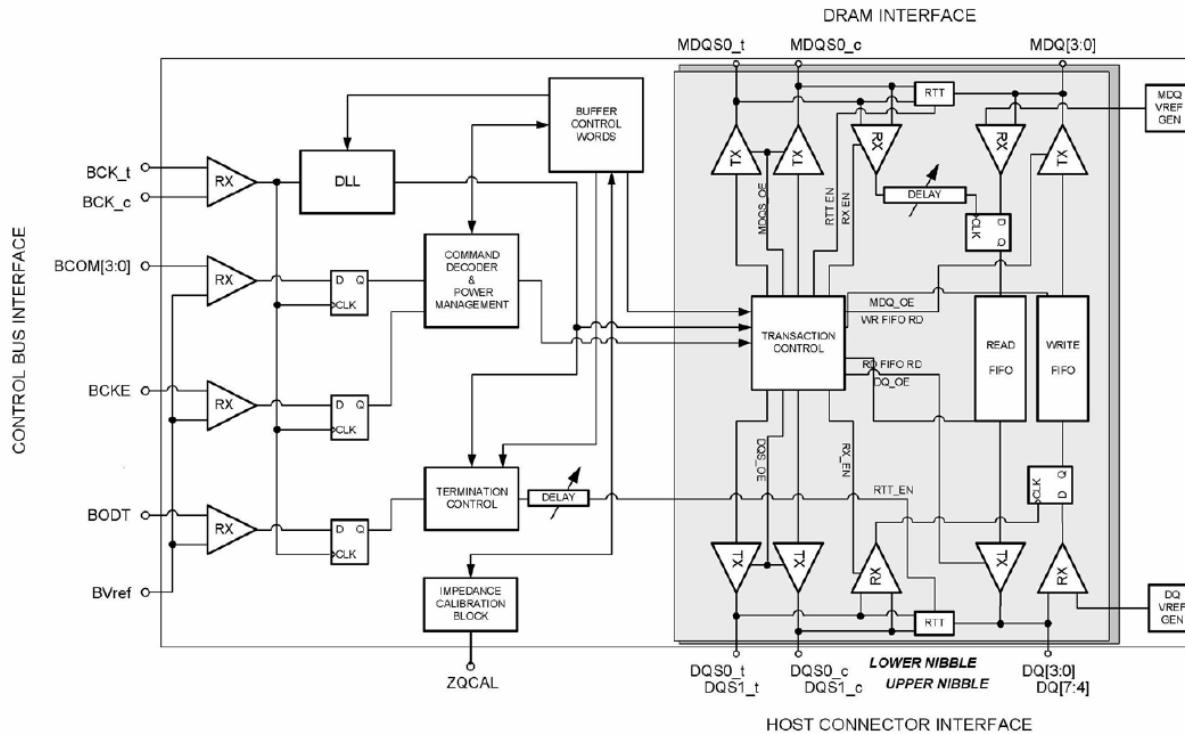
This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V VDD operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

See DDR4DB01 Standard

"a plurality of data handlers mounted on the PCB, wherein each respective data handler of the plurality of data handlers includes a data handler logic element, wherein each respective data handler of the plurality of data handlers is electrically coupled between a respective group of one or more memory devices and the connector, the respective group of one or more memory devices including at least one respective memory device in each of the one or more ranks;"

2.6 Logic Diagram

Figure 12 — Logic Diagram



See DDR4DB01 Standard.

"a plurality of data handlers mounted on the PCB, wherein each respective data handler of the plurality of data handlers includes a data handler logic element, wherein each respective data handler of the plurality of data handlers is electrically coupled between a respective group of one or more memory devices and the connector, the respective group of one or more memory devices including at least one respective memory device in each of the one or more ranks;"

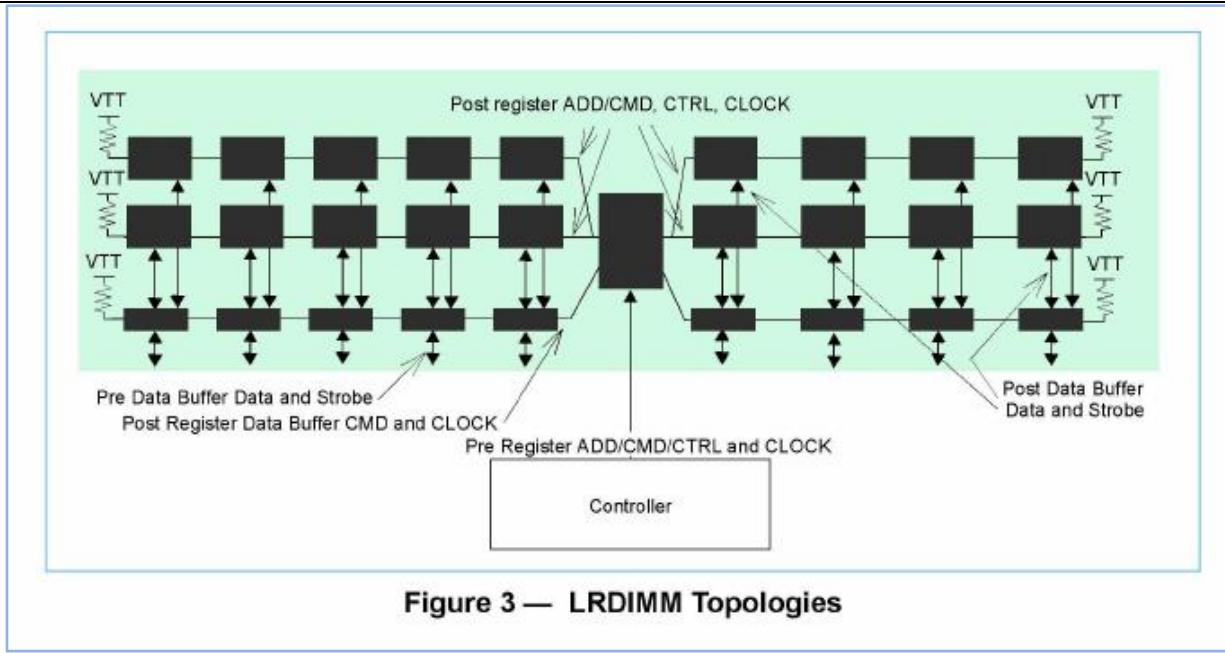


Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification.

"wherein the memory module is configurable to operate in any of at least a first mode and a second mode;"

<p>wherein the memory module is configurable to operate in any of at least a first mode and a second mode;</p>	<p>The SK hynix Product includes a memory module wherein the memory module is configurable to operate in any of at least a first mode and a second mode.</p> <p>For example, the SK hynix Products are operable in a first mode, e.g., a normal operating mode.</p> <div style="border: 1px solid black; padding: 10px; margin-top: 10px;"> <p style="text-align: center;">Table 35 — RC0C: Training Control Word</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #cccccc;"> <th colspan="4">Setting (DA[3:0])</th> <th>Definition</th> <th>Encoding</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">X</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td rowspan="10" style="vertical-align: middle; text-align: center;">Training mode selection</td><td>Normal operating mode</td></tr> <tr> <td style="text-align: center;">X</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td>Clock-to-CA training mode¹</td></tr> <tr> <td style="text-align: center;">X</td><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td>DCS0_n loopback mode¹</td></tr> <tr> <td style="text-align: center;">X</td><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td>DCS1_n loopback mode¹</td></tr> <tr> <td style="text-align: center;">X</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">0</td><td>DCKE0 loopback mode¹</td></tr> <tr> <td style="text-align: center;">X</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td style="text-align: center;">1</td><td>DCKE1 loopback mode¹</td></tr> <tr> <td style="text-align: center;">X</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">0</td><td>DODT0 loopback mode¹</td></tr> <tr> <td style="text-align: center;">X</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td style="text-align: center;">1</td><td>DODT1 loopback mode¹</td></tr> <tr> <td style="text-align: center;">0</td><td style="text-align: center;">X</td><td style="text-align: center;">X</td><td style="text-align: center;">X</td><td>Reserved</td></tr> <tr> <td style="text-align: center;">1</td><td style="text-align: center;">X</td><td style="text-align: center;">X</td><td style="text-align: center;">X</td><td>Reserved</td></tr> </tbody> </table> <p style="margin-top: 5px;">1. In these training modes the DDR4RCD01 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals).</p> <p>See JEDEC RCD01 Specification (annotations added).</p> <p>Further, the SK hynix Products are operable in a second mode, e.g., DB-to-DRAM Write Delay Training Mode.</p> </div>	Setting (DA[3:0])				Definition	Encoding	X	0	0	0	Training mode selection	Normal operating mode	X	0	0	1	Clock-to-CA training mode ¹	X	0	1	0	DCS0_n loopback mode ¹	X	0	1	1	DCS1_n loopback mode ¹	X	1	0	0	DCKE0 loopback mode ¹	X	1	0	1	DCKE1 loopback mode ¹	X	1	1	0	DODT0 loopback mode ¹	X	1	1	1	DODT1 loopback mode ¹	0	X	X	X	Reserved	1	X	X	X	Reserved
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0	X	X	X		Reserved																																																					
1	X	X	X		Reserved																																																					

"wherein the memory module is configurable to operate in any of at least a first mode and a second mode;"

2.1.8.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.

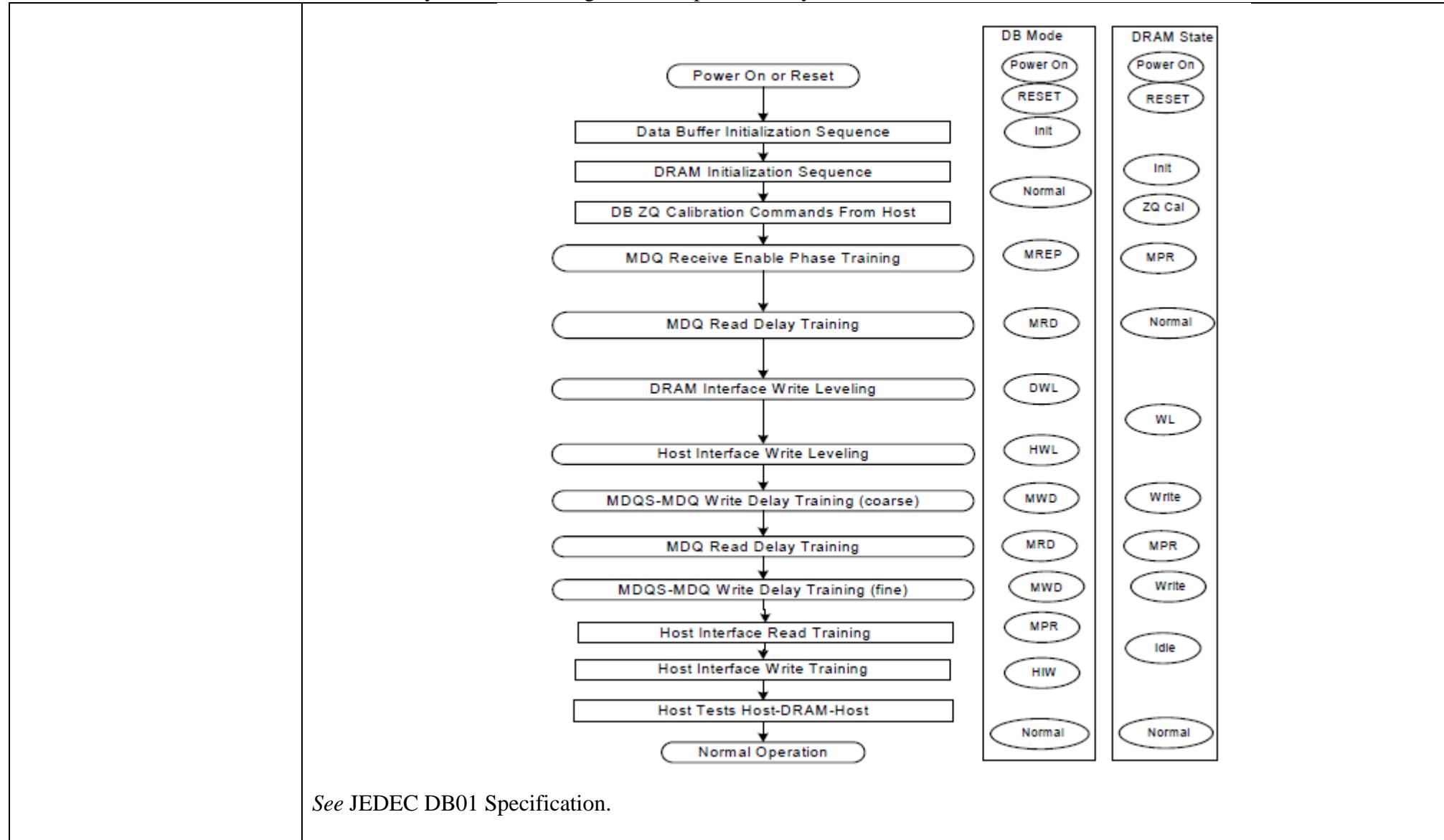
For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3 * 1/64 * t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

See JEDEC DB01 Specification.

The MWD mode is different than normal mode.

"wherein the memory module is configurable to operate in any of at least a first mode and a second mode;"



"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;

The SK hynix Product is operable in a first mode wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector.

The SK hynix Product is operable in a first mode wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations. For example, the SK hynix products include a control module that, in the first mode, is configured to receive system address and control signals from the system memory controller for memory read and write operations.



(Exemplary Photo of SK Hynix HMA84GL7AMR4N-UHTE)

The IDT RCD is configured to receive a set of input address and control signals corresponding to a memory read or write command information (e.g., CS, A0-A17, ACT, RAS, CAS, WE, CKE, etc.) from the memory controller.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

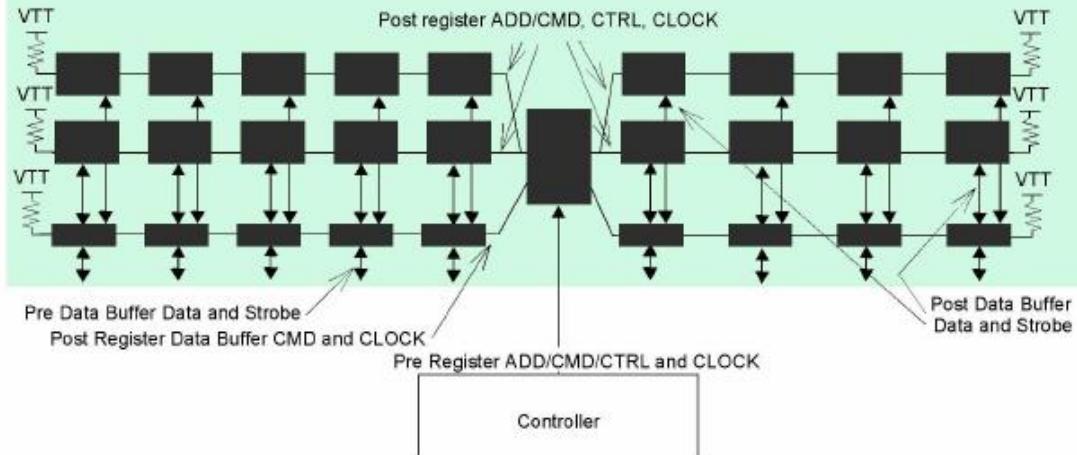


Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification at 1023NETLIST_00057109.

6.1 Signal Groups

This specification categorizes DDR4 SDRAM timing-critical signals into seven groups. Figure 3 summarizes the signals contained in each group. All signal groups, except Data, implement a fly-by topology. The signal groups are:

1. DQ and DQS signals connector to Data Buffer (DB)
2. DQ and DQS signals DB to SDRAM
3. PreRegister ADD/CMD and CTRL
4. PreRegister CK
5. PostRegister ADD/CMD
6. PostRegister Control
7. PostRegister CK
8. PostRegister BCOM, BODT, BCKE
9. PostRegister BCK

The PreRegister ADD/CMD and CTRL group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, PARITY, CSx_n, CKEx, and ODTx.

The PostRegister ADD/CMD group includes A0-A17, BA0-BA1, BG0-BG1, C0-C2, and PARITY.

The PostRegister CTRL group includes CSx_n, CKEx, and ODTx.

See JEDEC LRDIMM Specification at 1023NETLIST_00057109.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

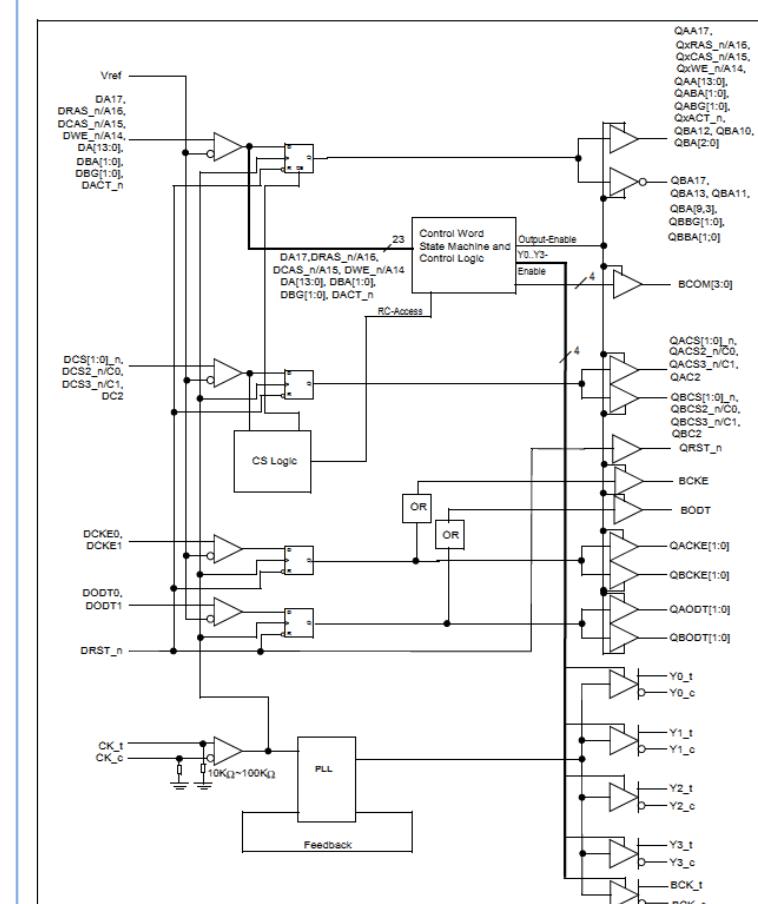
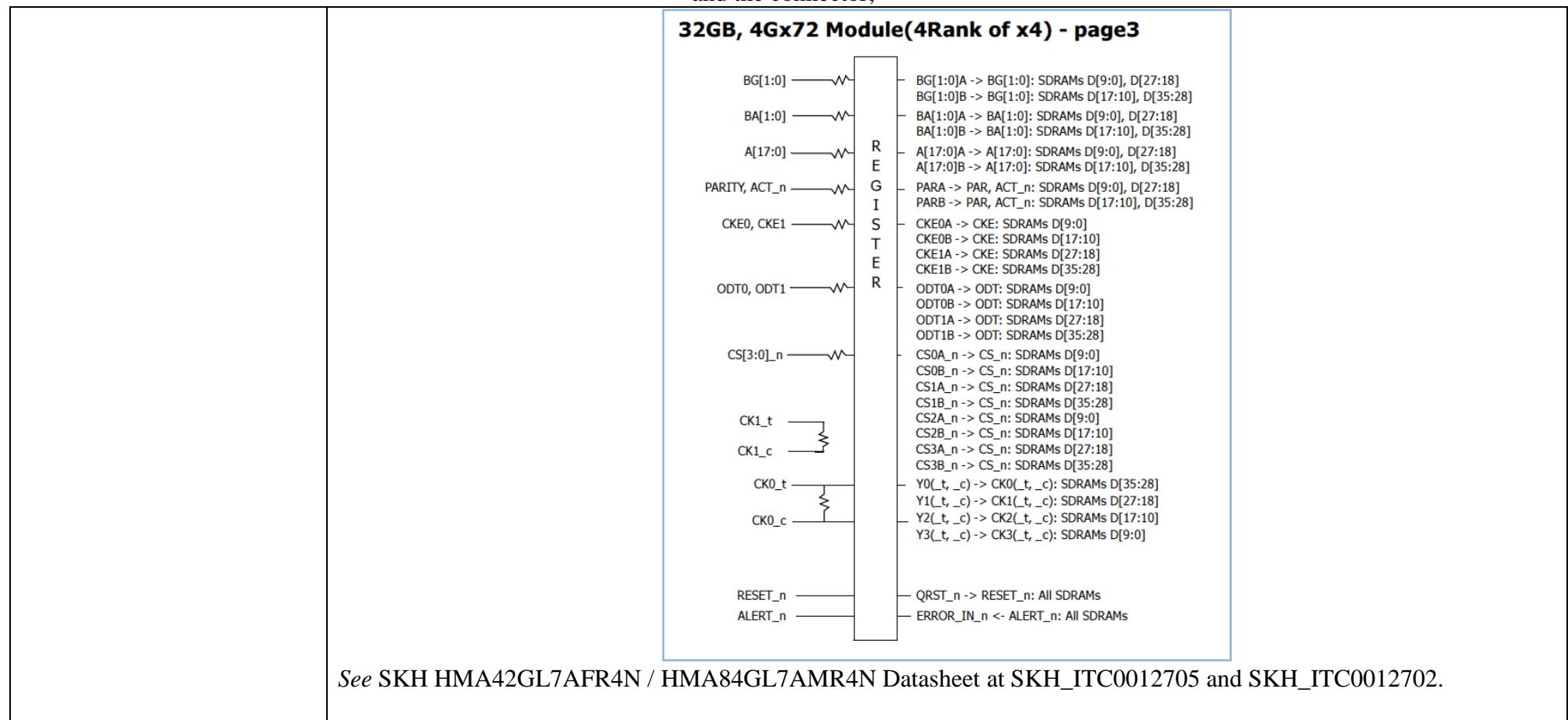


Figure 24 — Logic diagram (positive logic)

See JEDEC RCD01 Specification at SKH_JEDEC_0068343.

See also JEDEC RCD02 Specification at SKH_JEDEC_0068166.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"



"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

Table 4 — Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge, Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT, and CKE, are disabled during power-down. Input buffer, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. These pins are multi-function. For example, for activation with ACT_n Low, the pins are Addresses A16, A15, and A14, but for non-activation commands with ACT_n High, these are Command pins for Read, Write, and other commands defined in the command truth table
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15, and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH: no burst chop; LOW: burst chopped). See command truth table for details.

See JEDEC LRDIMM Specification at 1023NETLIST_00057100.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKEW1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n or DC0..DC1	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
Input Address and Command bus	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal.
	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
Clock inputs	CK_rCK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_rBCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

See JEDEC RCD01 Specification.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/I, QAODT0/I, QBCKE0/I, QBODT0/I QACS0_n, QACSI_n, QBCS0_n, QBCSI_n QACS2_n, QACSI3_n, QBCS2_n, QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS ²	Register output CKE and ODT signals. Register output Chip Select signals. Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1 QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input

See JEDEC RCD01 Specification.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 16 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n	CA15	CA14	WE_n	BG0	BG1	BA0	BA1	C2-C0	A12/BC_n	A13/A15	A10/AP	AD-AS	NOTE
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code		12					
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	V	V		
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	V	V	7,9	
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10	
Single Bank Precharge	PRE			H	H	L	H	L	BG	BA	V	V	V	V	L	V			
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	V	V	H	V		
RFU	RFU	H	H	L	H	L	H	H	RFU										
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)							
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	V	L	CA			
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA				
Write (BL8, on the Fly)	WRSS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA				
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	V	H	CA			
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA				
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA				
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	V	L	CA			
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA				
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA				
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	V	H	CA			
Read with Auto Pre-charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA				
Read with Auto Pre-charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA				
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	V	10		
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X		
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	6	
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	6	
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	V	H	V			
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	V	L	V			

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.6 Pinout Description		
Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/ A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DB/TDQS will provide the data mask function or Data Bus Inversion depending on MR5: A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert: It has multiple functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE: Input only pins (BG0-BG1,BAD-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

See JEDEC DDR4 DRAM Specification.

See also SKH HMA42GL7AFR4N / HMA84GL7AMR4N Datasheet at 6.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

	<p>2.2 Features and Functions</p> <p>The DDR4RCD01 has three basic modes of operation associated with the DA[1:0] bits in the DIMM Configuration Control Word (RC0D):</p> <ul style="list-style-type: none">• In Direct DualCS mode (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. The inputs pins DC[2:0] are forwarded to two sets of output pins, QAC[2:0] and QBC[2:0]. This is the normal operating mode ("QuadCS disabled" and "Encoded CS disabled").• In Direct QuadCS mode (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "QuadCS enabled" mode.• In Encoded QuadCS mode (DA[1:0] = 11), two copies of four output chip selects, i.e., QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the "Encoded QuadCS" mode. <p>In the two modes above the DDR4 register does not need to decode input signals to generate any chip select outputs.</p> <p><i>See JEDEC RCD01 Specification.</i></p>
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"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.9 Output Inversion Enabling/Disabling

Output Inversion is enabled by default, after DRST_n is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs. The DDR4 register output signals are divided into two classes: signals that can be inverted (e.g., regular addresses) and signals that cannot be inverted (because they have a special function), see Figure 18. Only the following 14 signals in the first class will be driven to the complement of the matching A-outputs: QBA3 to QBA9, QBA11, QBA13, QBA17, QBBA0 to QBBA1 and QBBG0 to QBBG1.

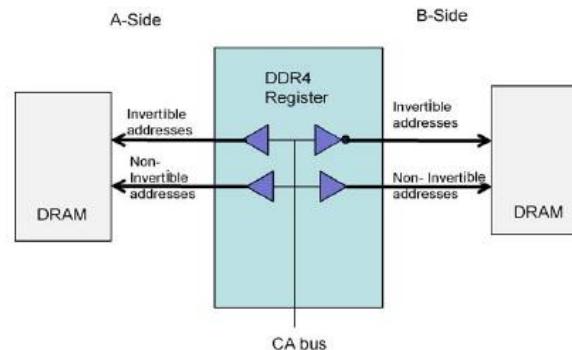


Figure 18 — Output Inversion Functional Diagram.

The Output Inversion feature is always enabled, even during DRAM MRS commands. In order to ensure that the DRAM receives the correct (i.e., uninverted) MRS bits, the host-to-register-to-DRAM MRS programming is split into a two-step process, see Figure 19. In the first step the A-side DRAMs are programmed using non-inverted addresses from the host. In the second step the B-side DRAMs are programmed using inverted addresses for the invertible address signals and non-inverted addresses for the non-invertible address signals from the host.

See JEDEC RCD01 Specification at SKH_JEDEC_0068328.

See also JEDEC RCD02 Specification at SKH_JEDEC_0068138.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.4 DDR4 SDRAM X4/8 Ballout using MO-207

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c ³				DM_n, DBI_n TDQS_t ² , (NC) ¹	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c	DQ1	VDDQ	ZQ				B
C	VDDQ	DQ0	DQS_t	VDD	VSS	VDDQ				C
D	VSSQ	DQ4 (NC) ¹	DQ2	DQ3	DQ5 (NC) ¹	VSSQ				D
E	VSS	VDDQ	DQ6 (NC) ¹	DQ7 (NC) ¹	VDDQ	VSS				E
F	VDD	(C2) ⁵ ODT1 ⁶	ODT	CK_t	CK_c	VDD				F
G	VSS	(C0) ⁵ CKE1 ⁶	CKE	CS_n	(C1) ⁵ (CS1_n) ⁶	TEN (NC) ⁷				G
H	VDD	WE_n A14	ACT_n	CAS_n A15	RAS_n A16	VSS				H
J	VREFCA	BG0	A10 AP	A12 BC_n	BG1	VDD				J
K	VSS	BA0	A4	A3	BA1	VSS				K
L	RESET_n	A6	A0	A1	A5	ALERT_n				L
M	VDD	A8	A2	A9	A7	VPP				M
N	VSS	A11	PAR	A17 (NC) ⁴	A13	VDD				N

NOTE 1 These pins are not connected for the X4 configuration.

NOTE 2 TDQS_t is not valid for the x4 configuration.

NOTE 3 TDQS_c is not valid for the x4 configuration.

NOTE 4 A17 is only defined for the x4 configuration.

NOTE 5 These pins are for stacked component such as 3DS. For mono package, these pins are NC.

NOTE 6 ODT1 / CKE1 /CS1_n are used together only for DDP.

NOTE 7 TEN is optional for 8Gb and above. This pin is not connected if TEN is not supported.

Figure 1 — DDR4 Ball Assignments for the x4/8 component

See JEDEC DDR4 SDRAM Specification.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.11 Latency Equalization Support

3D Stacked SDRAMs have a higher CAS latency than monolithic devices. For greater platform flexibility it is highly desirable to mix DIMMs with both 3DS and mono SDRAMs on the same DDR4 channel. Since memory controllers typically can only handle devices with equal CAS latencies in the same channel, it is required that the DDR4 register has a mechanism to increase the CAS latency of mono SDRAMs to match the CAS latency of 3DS SDRAMs. However, this mechanism only equalizes the DRAM latencies, not the total DIMM latencies. Hence this DDR4 register mechanism does not by itself allow mixing DDR4 RDIMMs and DDR4 LRDIMMs in the same channel.

To equalize different SDRAM latencies, the DDR4 register supports a programmable latency adder of 0 nCK, 1nCK, 2nCK, 3nCK or 4nCK for all DRAM commands, see conceptual diagram in Figure 2.12. The power-up default is 1nCK latency adder.

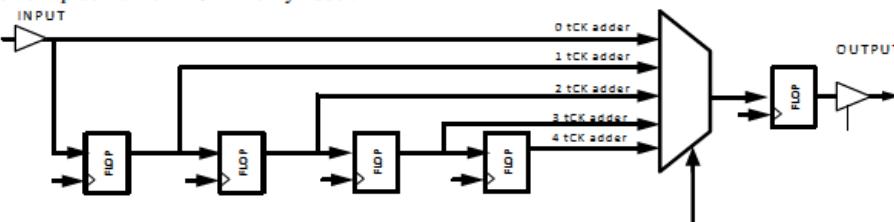


Figure 21 — Latency Equalizer Delays

See JEDEC RCD01 Specification.

See JEDEC RCD02 Specification.

2.5.2 Control Bus Timing

The output signals BCOM, BODT and BCKE are driven at the same time as the QxCA outputs, i.e., they are affected by the Command Latency Adder Control Word RC0F but a latency adder of 0 is not a valid configuration. For speeds above 2400MT/s, a minimum latency adder of 2 nCK is required in RC0F.

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

These signals are used during reads and writes that occur during operational mode, e.g., the first mode.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. **The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated** (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

JEDEC DDR4 SDRAM Specification (annotations added).

See also SKH DDR4 Device Operation at 7.

The SK hynix Products include data handlers that are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector. For example, the IDT Data Buffers propagate data signals between the memory devices and the system memory controller during read and write commands.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

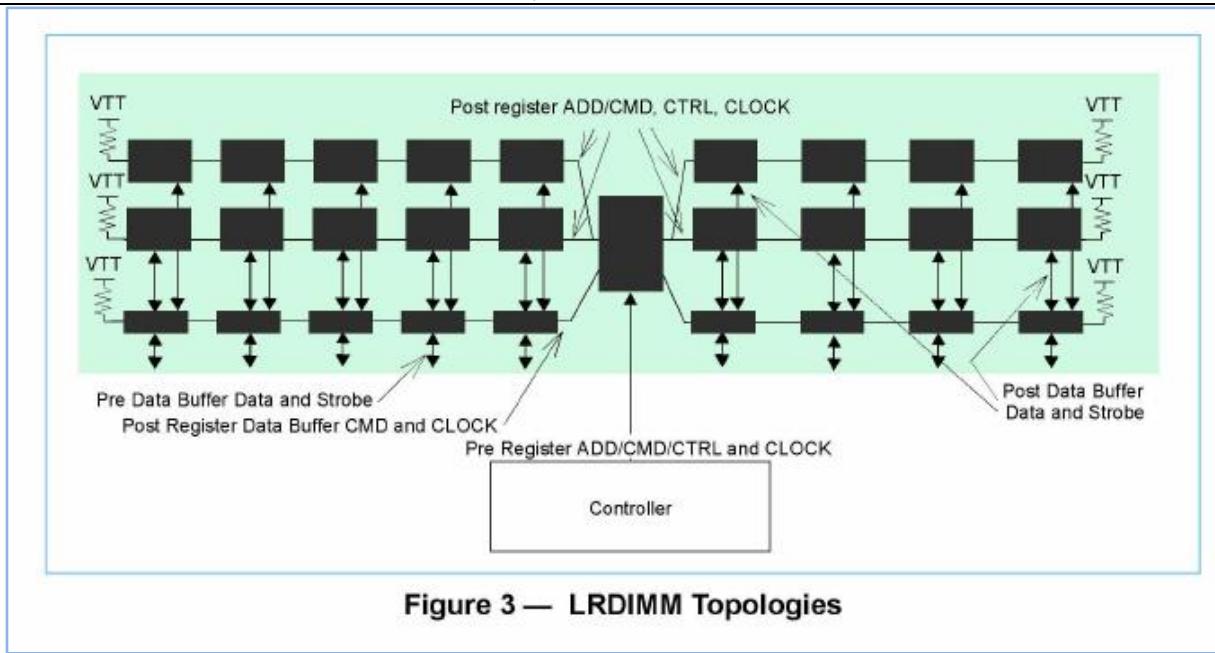


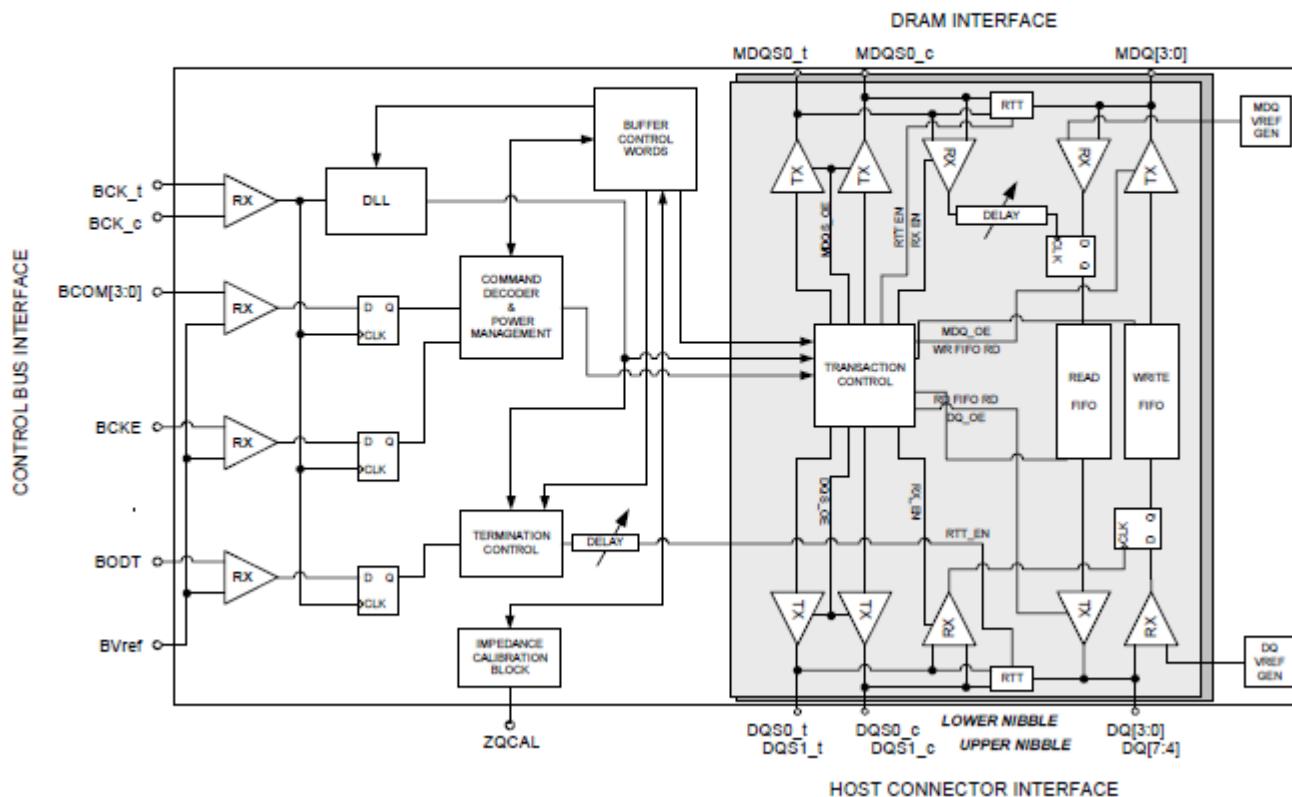
Figure 3 — LRDIMM Topologies

See JEDEC LRDIMM Specification.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.6 Logic Diagram

Figure 12 — Logic Diagram



See JEDEC DDR4 DB01 Standard Rev 1.0.

The propagated data signals are associated with memory read or write commands.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS2_n..DCS3_n or DC0..DC1	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
Input Address and Command bus	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal.
	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Data buffer control and communication outputs	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

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See JEDEC RCD01 Specification.

Table 16 — Terminal functions

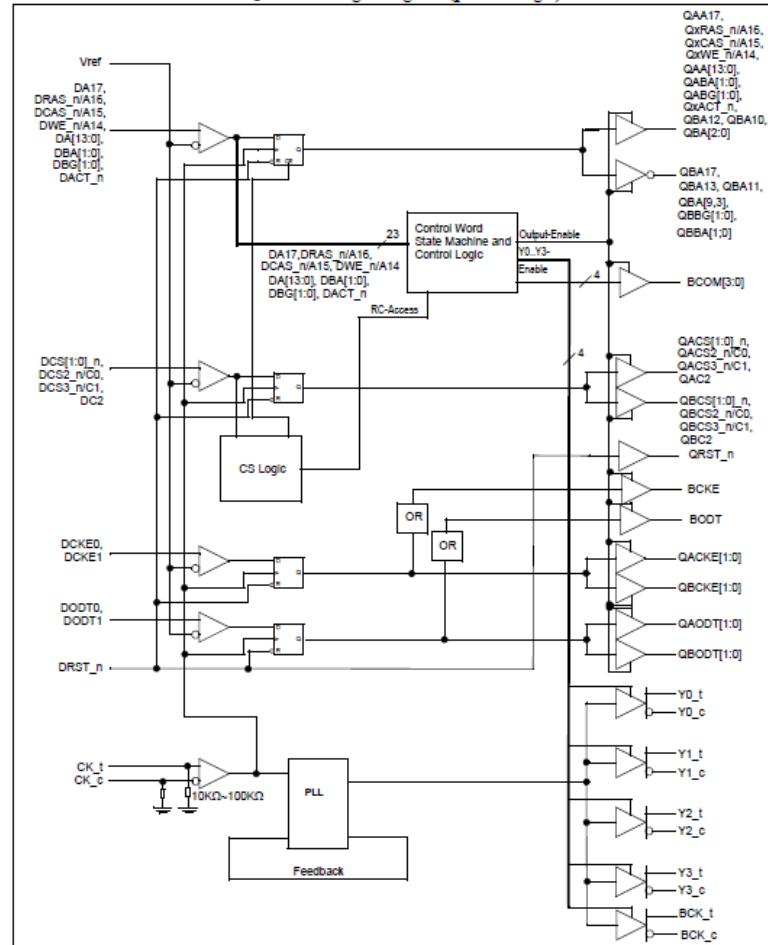
Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS ²	Register output CKE and ODT signals.
	QACS0_n, QACSI_n, QBCS0_n, QBCSI_n	CMOS ²	Register output Chip Select signals.
	QACS2_n, QACSI_n, QBCS2_n, QBCSI_n	CMOS ²	Register output Chip Select signals. These pins initiate DRAM address/command decodes.
	QAC0..QAC1, QBC0..QBC1		Some of these have alternative functions: <ul style="list-style-type: none"> QnCS2_n <=> QnC0 QnCS3_n <=> QnC1
Output Address and Command bus	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.
	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAGO..QAG1, QBG0..QBG1	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. <ul style="list-style-type: none"> QnA14 <=> QnWE_n QnA15 <=> QnCAS_n QnA16 <=> QnRAS_n
	QAACI_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4 RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.
I ² C Bus pins	SDA	Open drain I/O	I ² C Bus Data
	SCL	CMOS input ⁴	I ² C Bus Clock
	SA[2:0]	CMOS input ⁴	I ² C Bus Address signals
	BFUNC	CMOS input ⁵	Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register
	V _{DDSPD}	Power input	I ² C Bus power input

See JEDEC RCD01 Specification.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 16 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n	CA ₁₅	CA ₁₄	WE_n	BG	BA	V	OP Code			NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V					12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	V	L	V
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	V	H	V
RFU	RFU	H	H	L	H	L	H	H								RFU
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	V	L	CA
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRSS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	V	H	CA
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	V	L	CA
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	V	H	CA
Read with Auto Pre-charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Pre-charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	V	H	V
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	V	L	V

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.6 Pinout Description		
Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/ A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DB/TDQS will provide the data mask function or Data Bus Inversion depending on MR5: A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert: It has multiple functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE: Input only pins (BG0-BG1,BAD-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

See JEDEC DDR4 DRAM Specification.

Further, the RCD outputs signals via the BCOM to the DBs for Writes and Reads.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.1 Description

This dual 4-bit bidirectional data register with differential strobes is designed for 1.2 V VDD operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR4 Register. This interface consists of a 4-bit control bus, two dedicated control signals, a voltage reference input and a differential clock input.

All DQ inputs are pseudo-differential with an internal voltage reference. All DQ outputs are VDD terminated drivers optimized to drive single or dual terminated traces in DDR4 LRDIMM applications. The differential DQS strobes are used to sample the DQ inputs and are regenerated in the DDR4DB01 for driving out the DQ outputs on the opposite side of the device.

The clock inputs BCK_t and BCK_c are used to sample the control inputs BCOM[3:0], BCKE and BODT. The BCOM[3:0] inputs are used to write device internal control registers. The buffer control word (BCW) mechanism is described in more detail in Section 2.5.

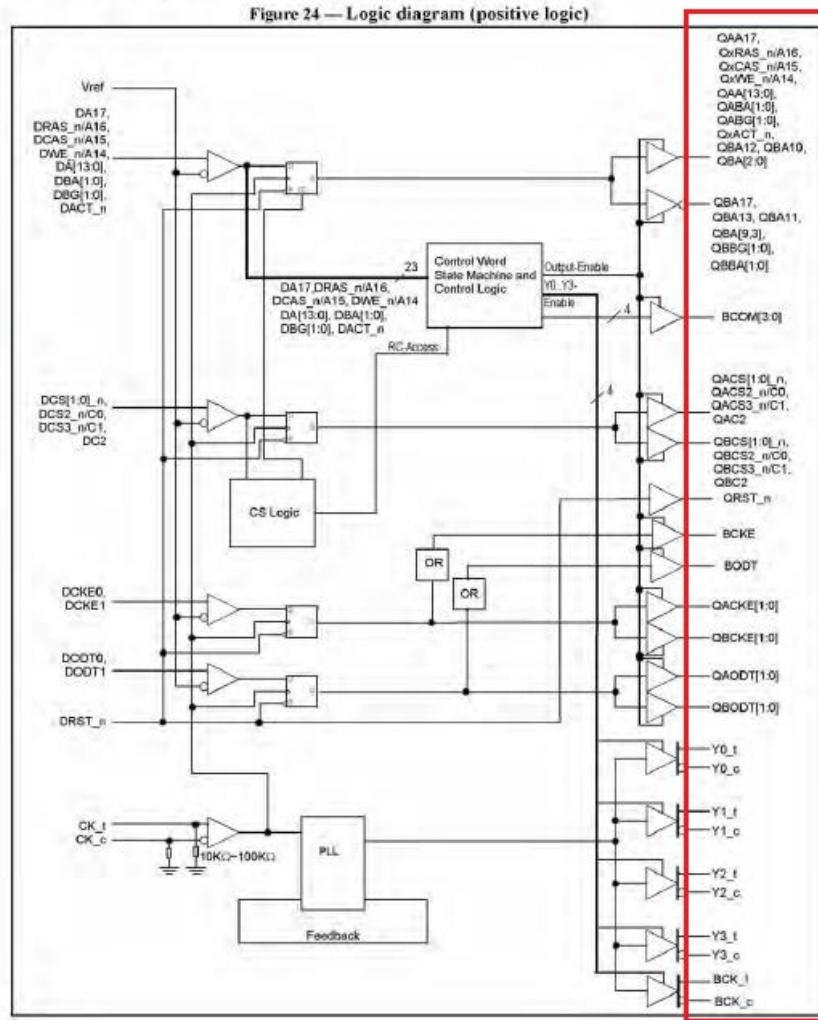
See DDR4DB01 Standard.

See also JEDEC DDR4 DB01 Standard Rev 1.0.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.17 Logic diagram

Figure 24 — Logic diagram (positive logic)



See DDR4RCD01 Standard.

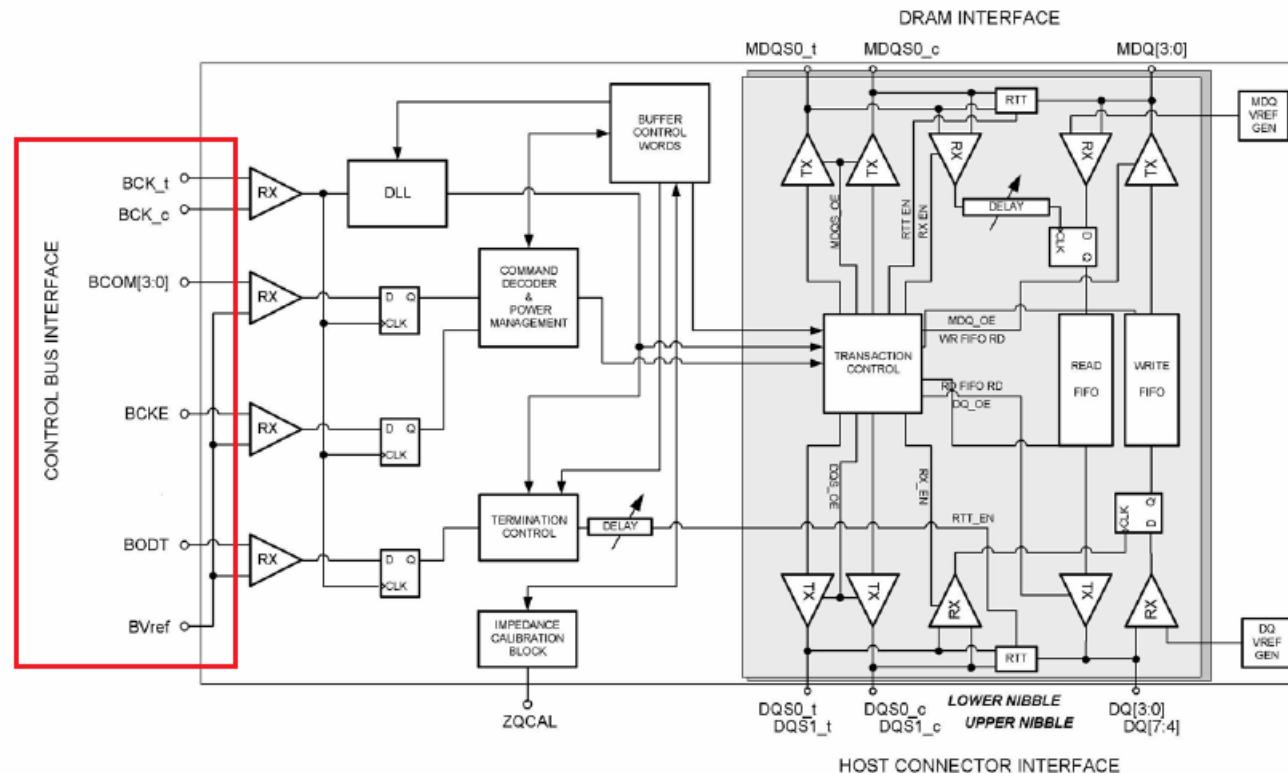
See JEDEC DDR4 RCD01 Standard Rev 1.0.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.17 Logic diagram

2.6 Logic Diagram

Figure 12 — Logic Diagram



See DDR4DB01 Standard.

See also JEDEC DDR4 DB01 Standard Rev 1.0.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

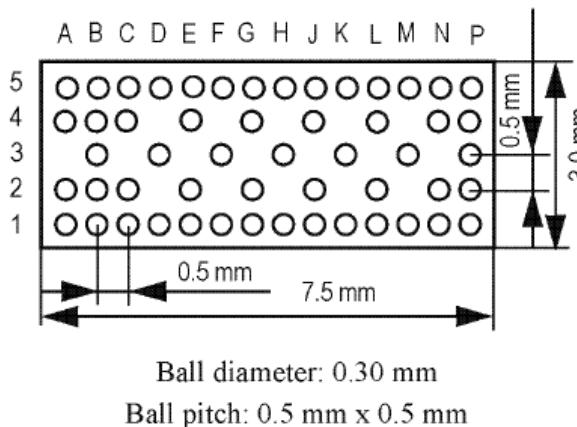


Figure 12 — 53 Ball Configuration 14 x5 (TOP VIEW)

Table 20 specifies the pinout for the DDR4DB02. The device has (mostly) symmetric pinout with host interface at the south side and DRAM interface at the north side.

Table 20 — Ball Assignment - 53-ball FBGA, 14 x 5 Grid, TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
5	BCOM3	BCOM2		MDQ3	MDQ2	MDQ7	MDQ6	MDQS0_t	MDQS0_c	MDQS1_c	MDQS1_t	MDQ1	MDQ0	MDQ5	MDQ4
4	BCOM0	BCOM1	V _{ss}		V _{ss}	ALERT_n									
3		V _{dd}		V _{dd}		V _{dd}		V _{dd}		V _{dd}		V _{dd}		BVrefCA	
2	BCK_t	BCKE	V _{ss}		V _{ss}	ZQCAL									
1	BCK_c	BODT	DQ3	DQ2	DQ7	DQ6	DQS0_t	DQS0_c	DQS1_c	DQS1_t	DQ1	DQ0	DQ5	DQ4	

See JEDEC BoD Ballot DDR4 DB02 Standard Rev 1.0.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.5 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DB). This interface is enabled on power-on and only disabled when the 'LRDIMM Disable' bit in the DIMM Configuration Control Word (RCD0) is set.

2.5.1 Control Bus Signals

Table 5 — List of Signals for Data Buffer control

Name	Description	Signal Count
BCOM[3:0]	Data buffer command signals	4
BCKE	Function of registered DCKE (dedicated non-encoded signal)	1
BODT	Function of registered DODT (dedicated non-encoded signal)	1
BCK_t, BCK_c	Clock outputs for the data buffers	2
BVrefCA	Reference voltage output for command and control signals connected to the data buffers	1
Total		9

See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.5.3 Control Bus Commands

2.5.3.1 Command List

Table 6 — Data Buffer Control Bus Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU ¹	Reserved for future use	1110
RFU ¹	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.5.4.1 Write Commands

Table 7 shows the sequence for write (WR4, WR8) commands. Each write command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. If CRC is enabled in the DRAM and in the DB (F4BC2x, DA7), the burst length will always be 10UI.

Table 7 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

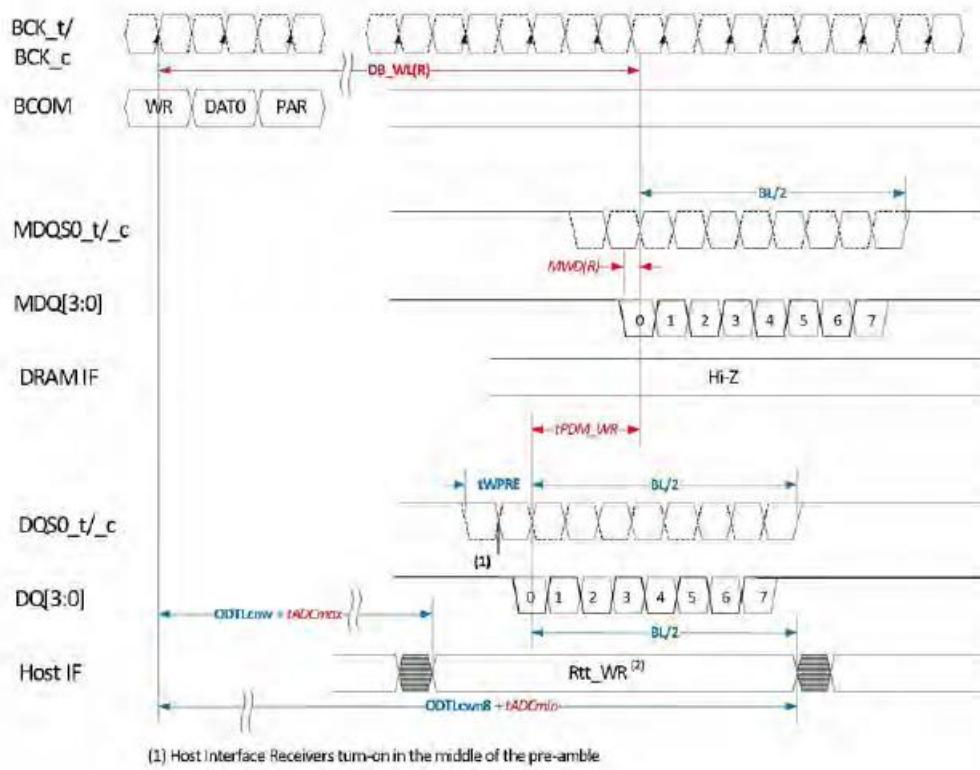


Figure 7 — WRITE Timing

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.5.5.2 Read Commands and MPR Override Reads

Table 8 shows the sequence for read (RD4, RD8) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MRO snoop register is set for fixed burst length of 8 or 4 (A[1:0] = '00' or '10').

Table 8 — Multicycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001

Table 8 — Multicycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Figure 8 shows the timing sequence for a Read command.

"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

Figure 8 shows the timing sequence for a Read command.

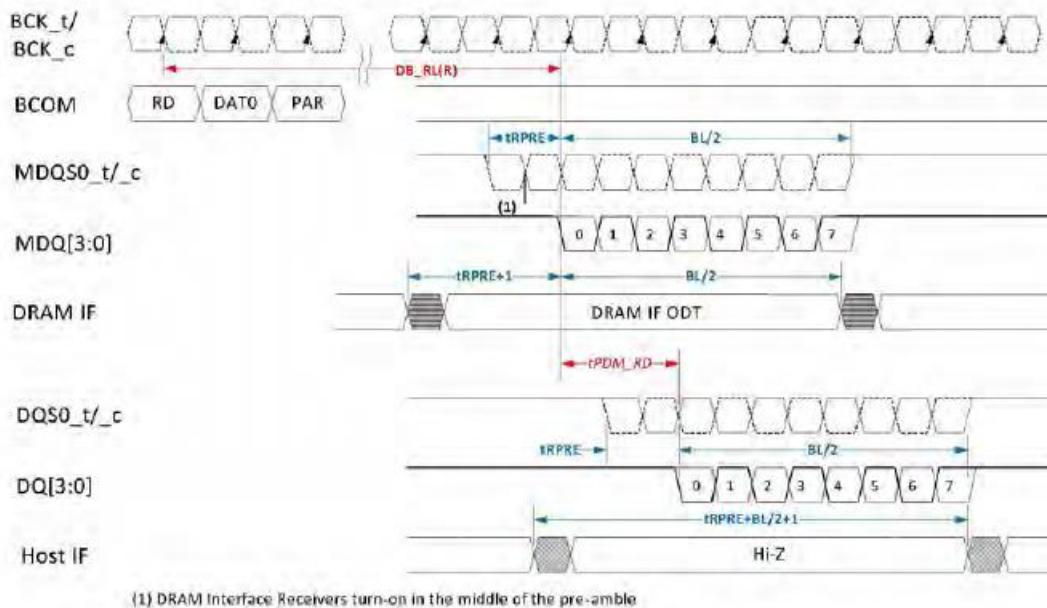


Figure 8—READ Timing

See JEDEC DDR4 RCD01Standard Rev 1.0.

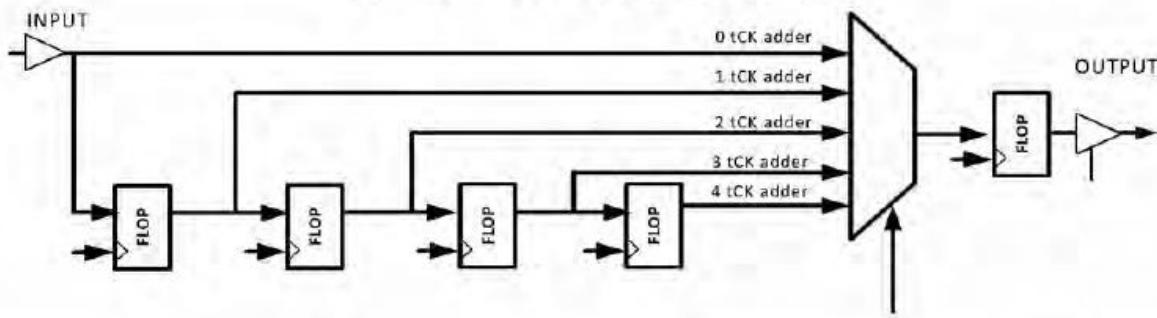
"wherein, in the first mode, the memory module is configured to be accessed by the system memory controller for memory read and write operations, and the data handlers are configured to propagate one or more data signals associated with the memory read or write operations between the memory devices and the connector;"

2.11 Latency Equalization Support

3D Stacked SDRAMs have a higher CAS latency than monolithic devices. For greater platform flexibility it is highly desirable to mix DIMMs with both 3DS and mono SDRAMs on the same DDR4 channel. Since memory controllers typically can only handle devices with equal CAS latencies in the same channel, it is required that the DDR4 register has a mechanism to increase the CAS latency of mono SDRAMs to match the CAS latency of 3DS SDRAMs. However, this mechanism only equalizes the DRAM latencies, not the total DIMM latencies. Hence this DDR4 register mechanism does not by itself allow mixing DDR4 RDIMMs and DDR4 LRDIMMs in the same channel.

To equalize different SDRAM latencies, the DDR4 register supports a programmable latency adder of 0 nCK, 1nCK, 2nCK, 3nCK or 4nCK for all DRAM commands - see conceptual diagram in Figure 2.12. The power-up default is 1nCK latency adder.

Figure 21 — Latency Equalizer Delays.



With a latency adder enabled, the DDR4 register will delay assertion of the QxCsN_n, QxCKEn, QxODTn, QxAn, QxBAn, QxBGn, QxACT_n, QxC2 and QxPAR outputs by the corresponding number of clock cycles.

See DDR4RCD01 Standard.

See JEDEC DDR4 RCD01 Standard Rev 1.0.

"wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module."

wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module.	<p>The SK hynix Product is operable in a second mode wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module.</p> <p>The SK hynix Product is operable in a second mode wherein, in the second mode, the memory devices are not accessed by the system memory controller. For example, in the second mode, the host-to-DB path is not used to perform read and write operations.</p>
---	--

"wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module."

2.1.8.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0]. UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable tunings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3 * 1/64 * tCK is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

See JEDEC DDR4 DB01 Standard Rev 1.0.

In the second mode, the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control

"wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module."

module. For example, the IDT data buffers transmit data signals to and from the data ports of the memory devices during DB-to-DRAM Write Delay mode according to BCW write and read commands (sent from the RCD), respectively.

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU ¹	Reserved for future use	1110
RFU ¹	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

"wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module."

2.5.5.4 BCW Write Command

Table 10 shows the sequence for buffer control word write commands.

Table 10 — Multicycle Sequence for BCW Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Write	Buffer control word write access command BCOM[3:0] = 1100
2	DAT0	First data transfer for BCW Write command BCOM[3:0] = {0, DA2, DA1, DA0}
3	DAT1	Second data transfer for BCW Write command BCOM[3:0] = {0, DA5, DA4, DA3}
4	DAT2	Third data transfer for BCW Write command BCOM[3:0] = {0, DA8, DA7, DA6}
5	DAT3	Fourth data transfer for BCW Write command BCOM[3:0] = {0, DA11, DA10, DA9}
6	DAT4	Fifth data transfer for BCW Write command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW writes BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW writes BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW writes BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW writes BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW writes BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW writes BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW writes BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW writes
7	PAR[3:0]	Even parity bits for BCW Write command and data PAR[x]: parity bit for 6 previous BCOM[x] transfers
8	Next Cmd	Next Command

"wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module."

The sequence for a BCW Write command is shown in Figure 10 below. The timing diagrams show how the BCW Write command is followed by five data transfer cycles and a parity data transfer cycle. Since the command sequence uses seven cycles it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the BCW Write command to the following valid command (also shown in the diagrams).

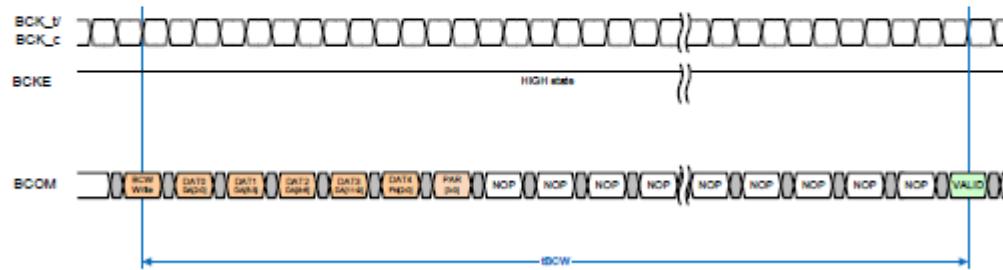


Figure 10 — Buffer Control Word Write command sequence

"wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module."

2.5.5.5 BCW Read Commands

The DDR4RCD01 generates a BCW Read command on the buffer control bus when it receives a CW Read command in RC06 with A12 = 1.

Table 11 shows the sequence for BCW Read commands.

Table 11 — Multicycle Sequence for BCW Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Read	Buffer control word read access command BCOM[3:0] = 1101
2	DAT0	First data transfer for BCW Read command BCOM[3:0] = {0, DA5, DA4, 0}
3	DAT1	Second data transfer for BCW Read command BCOM[3:0] = {0, DA8, DA7, DA6}
4	DAT2	Third data transfer for BCW Read command BCOM[3:0] = {0, DA11, DA10, DA9}
5	DAT3	Fourth data transfer for BCW Read command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW reads BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW reads BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW reads BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW reads BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW reads BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW reads BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW reads BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW reads
6	PAR[3:0]	Even parity bits for BCW Read command and data PAR[x]: parity bit for 5 previous BCOM[x] transfers
7	Next Cmd	Next Command

The sequence for BCW Read command is shown in Figure 11 below. The timing diagrams show how the BCW Read command is followed by four data transfer cycles and a parity data transfer cycle. This BCW Read command moves the selected BCW bits to MPR0 and configures the DB for MPR override read mode for the next Read command. The DB treats the first Read command after a BCW Read command as an MPR0 override read (regardless of the BCOM[1:0] bits during the DAT0 cycle of the corresponding BCOM Read command). The read data is driven out after DB_RL(R0) on the host interface DQ pins after the Read command. Just like in regular MPR override read mode, DDR4RCD01 will forward Read command to DRAM but DDR4DB01 will ignore read data from DRAM.

"wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module."

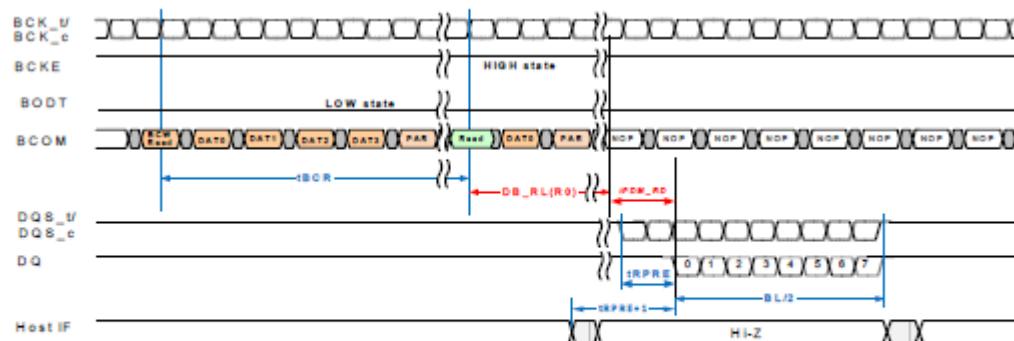


Figure 11 — BCW Read command sequence

See JEDEC DDR4 RCD01Standard Rev 1.0.

"wherein, in the second mode, the memory devices are not accessed by the system memory controller, and the data handler logic element in the each respective data handler is configured to provide respective data patterns to the respective group of one or more memory devices based on information output from the control module."

2.1.8.5 DB-to-DRAM Write Delay (MWD) Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.

MPRx[7:0] is driven to MDQ[7:0]. UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.

For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3 * 1/64 * tCK is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

See JEDEC DDR4 DB01 Standard Rev 1.0.

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	<p>The IDT RCD sends address and control signals (as part of the read and write commands) to the memory devices so that they can receive one or more data signals from the IDT Data Buffers during the second mode.</p> <p>2.1.8.5 DB-to-DRAM Write Delay (MWD) Training Mode</p> <p>For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from the data buffer's internal data control words that are written through the DDR4 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.</p> <p>To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay training mode in the Training Mode Control Word (BC0C) and it will also program the MPRs F5BC0x through F5BC3x and F6BC0x through F6BC3x. After that the host sends write commands to an arbitrary DRAM location without driving data on the host interface. The data for these write commands come from the DB MPRs.</p> <p>MPRx[7:0] is driven to MDQ[7:0], UIx, i.e. the content of MPR0 is driven out first and the content of MPR7 is driven out last.</p> <p>To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the data in the MPRs. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).</p> <p>The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words F[3:0]BC8x and F[3:0]BC9x for lower and upper nibble respectively. Since the DDR4DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively, the content of BC08 DA[1:0] is don't care while in this training mode. The nominal setting for F[3:0]BC8x/F[3:0]BC9x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including DWL (DRAM Interface Write Leveling) and HWL (Host Interface Write Leveling) when non-default settings are written into F[3:0]BC8x/F[3:0]BC9x.</p> <p>For higher DDR4 data rates, fine adjustment of the phase of individual bit lanes relative to MDQS may be required. For this purpose the host controller can utilize the per lane MDQ-MDQS write delay control words F[7:4]BCCx through F[7:4]BCFx. F4BCCx controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BCDx controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3 * 1/64 * tCK is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in F[3:0]BC8x or F[3:0]BC9x for the entire nibble.</p> <p>To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.</p> <p><i>See JEDEC DDR4 DB01 Standard Rev 1.0.</i></p>
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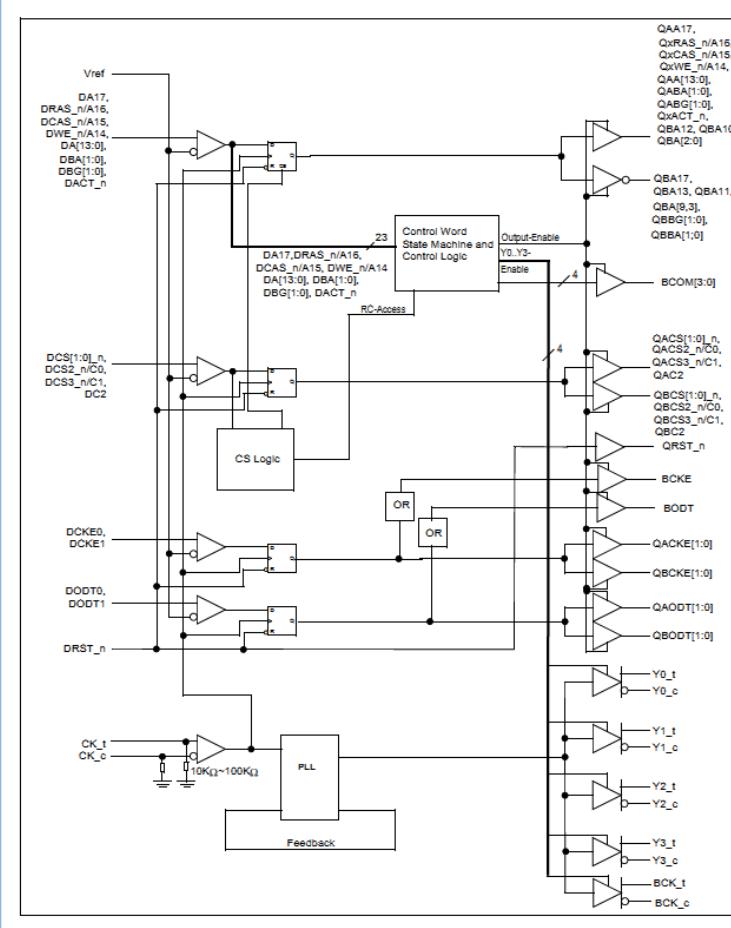


Figure 24 — Logic diagram (positive logic)

See JEDEC RCD01 Specification.

See also JEDEC RCD02 Specification.

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2.16 Terminal Functions Function tables

Table 16 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1	CMOS ¹ V _{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DODT0/1	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals.
	DCS0_n..DCS1_n	CMOS ¹ V _{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes.
	DCS1_n..DCS3_n or DC0..DC1	CMOS ¹ V _{REF} based	Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
Input Address and Command bus	DC2	CMOS ¹ V _{REF} based	DRAM corresponding register Chip ID 2 signal.
	DA0..DA13, DA17	CMOS ¹ V _{REF} based	DRAM corresponding register inputs.
	DBA0..DBA1, DBG0..DBG1	CMOS ¹ V _{REF} based	
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS ¹ V _{REF} based	In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS ¹ V _{REF} based	DRAM corresponding register DACT_n signal.
	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10KΩ~100KΩ pull-down resistor.
	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
	DPAR	CMOS ¹ V _{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Data buffer control and communication outputs	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
	BODT	CMOS ²	Data buffer on-die termination signal
	BCKE	CMOS ²	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS ²	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS ² differential	Differential clock output pair to the data buffer.
	BVrefCA	V _{DD} /2	Output reference voltage for data buffer control bus receivers

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	<p><i>See JEDEC RCD01 Specification.</i></p> <p style="text-align: center;">Table 16 — Terminal functions</p>			
Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS ²	Register output CKE and ODT signals.	
	QACS0_n, QACSI_n, QBCS0_n, QBCSI_n	CMOS ²	Register output Chip Select signals.	
	QACS2_n, QACSI_n, QBCS2_n, QBCSI_n	CMOS ²	Register output Chip Select signals. These pins initiate DRAM address/command decodes.	
	QAC0..QAC1, QBC0..QBC1		Some of these have alternative functions: <ul style="list-style-type: none"> • QnCS2_n <=> QnC0 • QnCS3_n <=> QnC1 	
	QAC2, QBC2	CMOS ²	Register output Chip ID2 signals.	
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAGO..QAG1, QBG0..QBG1	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.	
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. <ul style="list-style-type: none"> • QnA14 <=> QnWE_n • QnA15 <=> QnCAS_n • QnA16 <=> QnRAS_n 	
	QAACI_n, QBACT_n	CMOS ²	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.	
Vref output	QVrefCA	V _{DD} /2	Output reference voltage for DRAM receivers	
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c	CMOS ² differential	Redriven clock	
Reset output	QRST_n	CMOS ²	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4 RCD01 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.	
Parity outputs	QAPAR, QBPAR	CMOS ²	Redriven parity ³	
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.	
I ² C Bus pins	SDA SCL SA[2:0] BFUNC V _{DDSPD}	Open drain I/O CMOS input ⁴ CMOS input ⁴ CMOS input ⁵ Power input	I ² C Bus Data I ² C Bus Clock I ² C Bus Address signals Function pin. BFUNC=V _{SS} for primary register, BFUNC=V _{DD} for secondary register I ² C Bus power input	

See JEDEC RCD01 Specification.

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4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table

(b) Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 16 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n	CA ₁₅	WE_n	BG-BG1	BA-BA1	C2-C0	A12/ BC_n	A13/ A15	A10/ AP	AD-AS	NOTE
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code		12		
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
Single Bank Precharge	PRE			L	H	L	H	L	BG	BA	V	V	V	V	L	V
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	V	H	V
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)		BG	BA	V	Row Address (RA)					
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRSS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Pre-charge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Pre-charge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Pre-charge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	V	L	CA
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Pre-charge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Pre-charge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Pre-charge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

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2.6 Pinout Description		
Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/ A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V _{DD} .

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Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQSL_c. When disabled via mode register A11 = 0 in MR1, DM/DB/TDQS will provide the data mask function or Data Bus Inversion depending on MR5: A11,12,10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert: It has multiple functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE: Input only pins (BG0-BG1,BAD-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

See JEDEC DDR4 DRAM Specification.